# SIXTH INTERIM PROGRESS REPORT
# ON THE PHYSICAL REALIZATION OF AN ELECTRONIC COMPUTING INSTRUMENT

by

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THE INSTITUTE FOR ADVANCED STUDY
ELECTRONIC COMPUTER PROJECT
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# PREFACE

This report has been prepared under the terms of Contracts W-36-034-ORD-7481 and DA-36-034-ORD-19 between the Research and Development Service, U. S. Army Ordnance Corps and the Institute for Advanced Study. It is both a final report on the work undertaken under the former contract and an interim report under the latter one, describing the progress up to January 1, 1951.

The Institute for Advanced Study was particularly fortunate in having Dr. C. V. L. Smith, the head of the Computer Branch of the Office of Naval Research prepare this report, and the personnel of the Computer Project wish to express their gratitude to him for undertaking this onerous task and for completing it in such an excellent fashion.

Since this report was written certain changes have been made in some of the circuits described herein and certain other organs, notably the Control, have been designed. These will be discussed in a subsequent report.

John von Neumann
Project Director

Institute for Advanced Study

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# INTRODUCTION

I was fortunate in finding it possible to spend the period from July 1950 to February 1951 at the Electronic Computer Project of the Institute for Advanced Study, engaged in studying the logical organization and the engineering development of the computer. From my observations I have written the following report, which is intended to present the status of the computer development as of January 1, 1951.

As the Control Organ was not completed at that date, the reader must expect to find certain omissions in my account of the other Organs, particularly as regards those circuits necessary to interconnect them into a complete system. Apart from this, the account of the Arithmetic Organ and of the Memory are reasonably complete, while substantial portions of the Control are also described. It must be emphasized that modifications will be required in the existing circuitry as the Control is completed: these, however, will be ordinarily in matters of detail rather than in overall organization.

I have not attempted to describe the physical lay-out of the computer, as this has been done in earlier reports. The reader is referred to these for overall organization and for details of the elegant and ingenious three-dimensional organization of the individual chassis. I have concentrated my attention on the circuits, and endeavored to explain their operation in some detail.

Obviously it would have been impossible for me to write this report

without the active co-operation of the members of the staff of the Project. I thank them collectively and individually for their patience in answering my questions and helping me to clarify my understanding of their work.

CHARLES V. L. SMITH

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## I. CIRCUIT ELEMENTS

Before proceeding to describe the organization of the various organs of the computer in detail, we will first give a brief discussion of some basic circuits which occur repeatedly.

First, and most important, is the familiar Eccles-Jordan circuit, the form used being illustrated in Fig. 1. This will always be referred to as a "toggle".

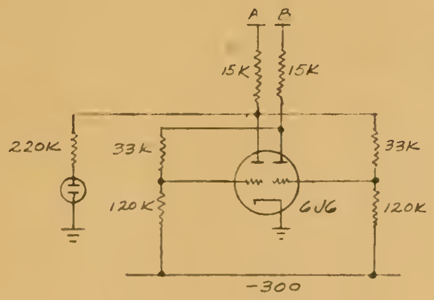


Fig. 1.

A and B designate d. c. buses: these are held at +150v except when clearing action is desired, when the appropriate voltage is dropped to +50v, this will be discussed below.

The circuit is so designed that satisfactory operation is obtained if the resistor values do not vary more than 10% from their nominal values and the tube characteristics remain within the region where the ordinates lie

between 50% and 200% of their nominal values.

If nominal values of the resistors are used, and the 6J6 characteristics as given by the manufacturer, the following electrode voltages obtain:

| | |
|---|---|
| "on" grid | +.5v |
| "off" grid | -40v |
| "on" plate | +35v |
| "off" plate | +100v |
| "on" grid current | .6ma. |

A conventional representation of the toggle circuit is sometimes convenient: the one given in Fig. 2 will sometimes be used

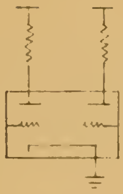


Fig. 2.

The toggle is a binary device, in the sense that at all times one section of the 6J6 is in a conducting state, while the other is not. It is merely a matter of convenience which one of the two states is chosen to represent a binary 0, the other then necessarily representing a binary 1. In order to represent visually the contents of a toggle, a neon bulb is connected from the plate of the section that is off when the toggle is holding a 1 to ground. Clearly this bulb lights up to represent 1, while it is off when the toggle holds 0. Thus in Fig. 1 we have adopted the convention that

the toggle holds a 1 when the left-hand section is non-conducting.

We now consider the "clearing" action, assuming the given convention as to the contents of the toggle. Suppose the toggle to hold a 0, and let bus A drop to +50v, while B remains at +150v. The grid voltage of the right section is merely reduced still further. Hence that section remains cut off, the grid voltage of this left section is held up, and the state of the toggle does not change. On the other hand, if bus B is dropped to +50v, while A is maintained at +150v, the grid voltage of the left-hand section is reduced below cut-off, and the toggle is changed to its other state. Similarly, if a 1 is held, dropping B to +50v while holding A at +150v has no effect, while dropping A to +50v while holding B at +150v changes the state of the toggle.

Putting this differently, the operation of dropping A to +50v while holding B at +150v guarantees that the toggle will subsequently hold a 0, while holding A at +150v and dropping B to +50v guarantees that it will subsequently hold a 1. Thus these operations are respectively referred to as "clearing to 0" and "clearing to 1". The clearing action is produced by pulsing the appropriate bus. With the present toggles, it is necessary that the bus voltage should remain below +70v for approximately one microsecond to produce the desired clearing.

In a few places in the computer, it is desired to use a toggle which requires a shorter time to change from one state to the other. In these applications a so-called "super-toggle" is used, which changes its state in half the time required by the ordinary toggle. The circuit is given in Fig. 3.

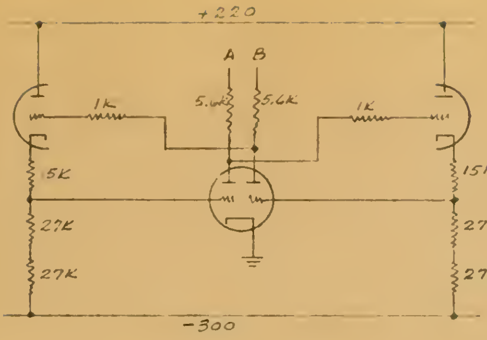


Fig. 3.

It has been shown how a toggle may be set in a desired state, or "cleared". It is also necessary to be able to set a toggle into the same state as another toggle: that is, given toggles A and B, it is necessary to provide a mechanism which guarantees that, after some definite time, the contents of A are identical with those of B. This is readily accomplished by means of a gate circuit as shown in Fig. 4.

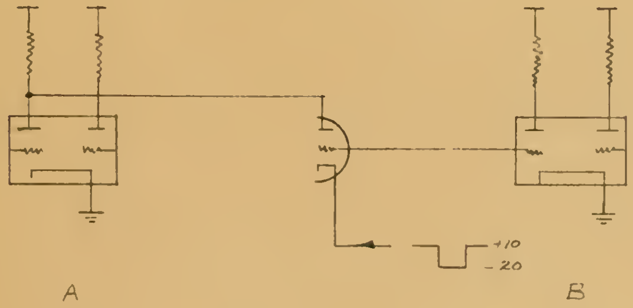


Fig. 4.

The tube used here is one section of a 6J6, with cathode normally maintained at +10v. When it is desired to transfer information from B to A (note that the given circuit permits a transfer to be made only in this direction), the cathode of the gate is dropped to -20v. The gate cannot conduct while its cathode is held at +10v, as its grid cannot be above about +.5v. Let us use our earlier convention as to the representation of binary 0's and 1's by states of the toggle. If B holds a 1, clearly nothing can happen when the gating signal arrives at the cathode of the gate, as this tube must remain cut off. If, on the other hand, B holds a 0, conduction takes place when the cathode of the gate falls to -20v, and plate current, flowing through the plate load resistor of the left section of A, will cause A to assume the state representing 0. The gate thus guarantees that if B holds a 0 at the time the gating signal is applied, A will be caused to hold a 0. Suppose now that before the arrival of the gating signal, A is cleared to 1. Then if B holds a 0, the gate causes A to assume the 0 state, while if B holds a 1, the gate has no effect, and A continues to hold a 1. Thus the sequence of signals "clear A to 1" and "open gate into A", results in A holding the same information as B.

We also note that if the gating signal were made sufficiently negative, enough grid current could be drawn by the gate to cause a change of state in B. This effect is not used in the present design, but could conceivably be useful.

The gate circuit as described is a coincidence device, equivalent to the formation of a logical product. Other methods are used in parts of the machine; for example, consider the circuit of Fig. 5, where the signals applied to the grids assume the levels of +10v or -10v. This is a cathode

follower, and the cathode will follow the highest grid. Thus the cathode voltage will assume the lower level if and only if both grid voltages assume their lower levels.

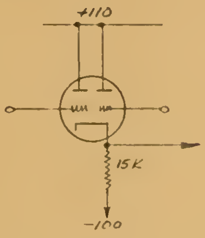


Fig. 5.

Another gate circuit which will be found in the computer makes use of two diodes connected as in Fig. 6. (see for example DWG 1325).

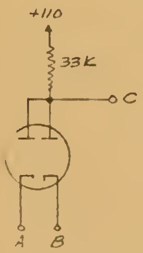


Fig. 6.

In one particular case A assumes one of two levels (+10v, -20v) and B also one of two levels (+10v, -10v). The voltage at C will always be slightly above that of the lower cathode, and hence will assume a high value (slightly above +10v) only if both A and B simultaneously attain their higher values.

Usually we think of one input to a gate as an enabling signal, which places the gate in a condition to pass on the other input. A convenient symbol for a gate is given in Fig. 7,

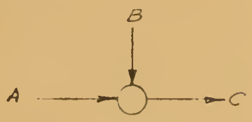


Fig. 7.

Where A and B are the inputs and C the output; the enabling signal is B. Sometimes it is convenient to use a solid arrowhead for a static voltage, and reserve the open arrowhead for a voltage pulse.

Cathode followers are found in considerable numbers. These are used, for example, to drive a number of gates of the type illustrated in Fig. 4, and in other places where it is necessary to supply a considerable amount of current from a low impedance source. The cathode followers are ordinarily operated in that region of the characteristics, where sufficient plate current is drawn to cause the cathode voltage to rise slightly above the grid voltage, so that no grid current flows. For purposes of ordinary analysis, we shall commonly assume that the cathode voltage is exactly the same as that of the grid, the cathode rise being neglected. This will ordinarily not lead to any difficulties.

# II. THE ARITHMETIC ORGAN

## THE REGISTERS

A Register is essentially merely a device which serves as the repository of a single word of machine language. The term is usually used to designate a storage device the contents of which are directly available with very slight delay. Thus in a machine whose language consists of forty bit words, a set of forty toggles forms a convenient Register. However, mere storage of information does not suffice, as the Registers which are to serve as the Accumulator and the AR and SR Registers of the machine must be capable of other functions. These devices must be able to transmit and receive information, and to perform shifts (at least for certain purposes) of the information to the left or to the right.

The transmission of information into or out of a Register consisting of toggles is readily accomplished by the gating circuits that have already been discussed, while the simple means by which toggles can be cleared to 1 or to 0 have also been described.

In performing the shifting operation, it is desired that the information should never exist as merely transitory electric or magnetic fields, but should rather at all times exist in static form. An effective method of accomplishing this is as follows: two rows of toggles are provided-in the Registers of the machine the two rows (upper and lower) in Register RI are called $R^1$ and $R_1$, and similarly for the other two Registers-and gates are arranged whereby the information held in a toggle of the lower row is transmitted to the left or right in two steps: first, up to the corresponding toggle of the upper row, then second, from this toggle down to the left

or to the right. Fig. 8 shows how this is done: it represents the columns n-1, n, and n+1 of the Register.

Two gates lead up from each toggle of the lower row to the toggle in the corresponding position of the upper row, while from each toggle in the upper row a gate leads down to the toggles in adjacent columns of the lower row. The gate G(reen) can transmit a 0 up, while Y(ellow) can transmit a 1. Hence to assure the transmission of the number in the lower row of toggles to the upper row, two alternative procedures are at our disposal: the top row may first be cleared to 0 and then the Yellow gates opened, or the top row may be first cleared to 1 and then the Green gates opened.

To shift the number now standing in the top row of toggles back down to the lower row, in such a way that the resulting contents of the lower row will be the number that originally resided in that row, but shifted one place to the right or to the left, is the function of the gates R(ed) and B(lack). For the right shift, the Black gates alone are available: from the diagram, it is clear that these can transmit only 1's, so that it is necessary first to clear the lower row to 0's before opening the Black gates. For the left shift, the Red gates can transmit only 0's, so it is necessary first to clear the lower row to 1's.

It was shown in the discussion of gates, that it is quite possible to cause a gate tube to clear the toggle from which it transmits information. Thus the Green gates could be used to clear the toggles of the bottom row to 1's, while the Yellow gates could be used to clear these toggles to 0's. Similarly, the Red gates could be used to clear the toggles of the upper row to 1's, while the Black gates could be used to clear these toggles to 0's. Although this property of the gate tubes is not exploited in the

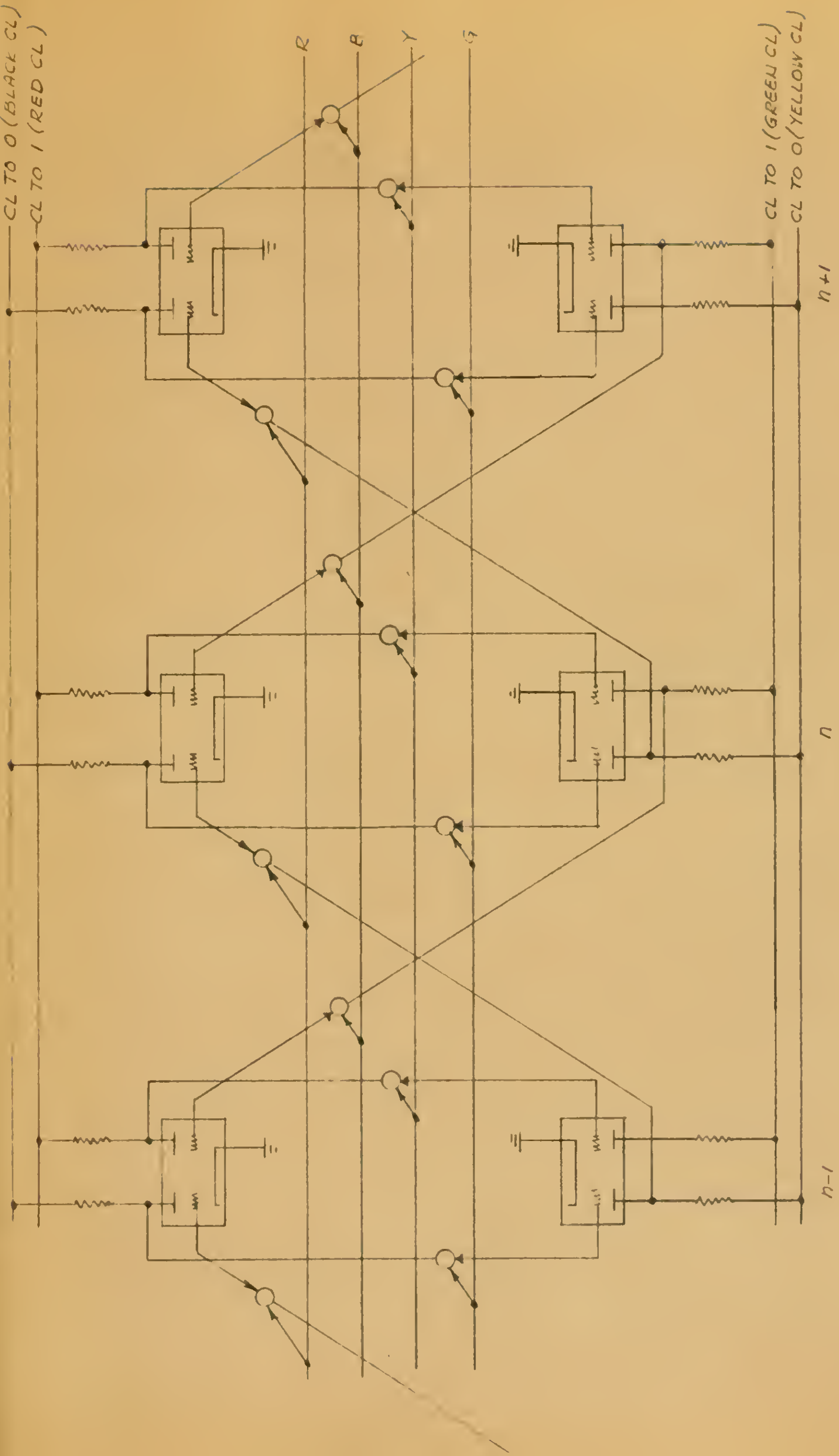

CL TO 0 (BLACK CL)
CL TO 1 (RED CL)
R
B
Y
G
CL TO 1 (GREEN CL)
CL TO 0 (YELLOW CL)
n+1
n
n-1

Figure 8

present machine, it nevertheless provides a convenient manner of designating the various clear operations. Thus a clear will be described by the color used to designate that gate which could be used to perform the clear. The following table shows how the color code is used to describe the various shift and clear operations:

Red: Shift left down zero
Clear top to one.

Green: Shift up zero
Clear bottom to one.

Yellow: Shift up one
Clear Bottom to zero.

Black: Shift right down one
Clear top to zero.

In this terminology, the process of shifting right one place consists of the following operations: Black clear, Yellow gate, Yellow clear, Black gate. The left shift is described by: Black clear, Yellow gate, Green clear, Red gate. In each case, of course, there is an alternative process available which makes use of the Green shift up.

The structure of a forty stage Shifting Register follows directly from the diagram of the three stages which has been discussed. The actual Shifting Registers in the machine all differ in certain details from the one described, which may be thought of as an archtype. It is clear that means must be provided by which information can be inserted in or extracted from the Registers. This is done by changing certain of the connections to the gates. Registers RI and RII remain Shifting Registers with these special connections. RIII, on the other hand, should not be thought of as a Shifting Register at all. The two rows of toggles in RIII actually form two independent Registers, which form part of the means of communication between the

Williams Memory and the rest of the machine. Also a small amount of additional equipment is associated with the various Registers. In the interests of clarity, each of the three Registers will be briefly discussed and the interconnections with the rest of the machine indicated.

All three Registers consist physically of four chassis, each of which contains four rows of tubes, laid out as follows:

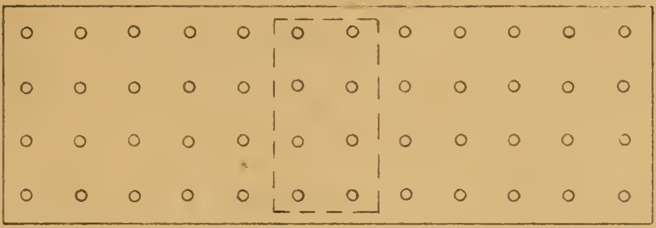


Fig. 9.

All tubes in the chassis are 6J6's except for those enclosed by the dotted rectangle, which are 5687's. In the first and fourth rows, the first five and the last five tubes are toggles. In the second and third rows, the first and last five tubes are gates - actually each tube is a pair of gates. The tubes enclosed by the dotted rectangle are cathode followers used as gate drivers. The two in any row are connected in parallel, and serve to drive five 6J6 gate tubes.

In each chassis, suppose the columns of tubes, exclusive of those within the dotted rectangle, to be numbered n, n+1, ..., n+9, where n = 0, 10, 20, 30 for the four chassis, respectively. Since numbers are represented in the machine with decimal point at the left, it is convenient to refer to any stage of a Register as $2^{-n}$, $2^0$ being the "sign digit".

RI and RII are identical except for certain circuits exterior to the Register Chassis: these will be described later. A schematic is given in DWG No. 1322. It has already been observed that RIII is not a Shifting Register at all. It actually consists of two Registers and associated gate tubes by means of which information can be inserted in $R^3$ and $R_3$: for a schematic, see DWG No. 1323, in which the top row of tubes shown are the Complement Gates used to read out to the Adder, and are not actually mounted on the Register Chassis. Despite these differences, it is convenient to use the same nomenclature for the gate tubes of all three Registers. In all cases, the row of tubes directly below the toggles of $R^k$ are alternately from the left end of the chassis Red and Black gates, while those of the row below are alternately Yellow and Green gates. Each gate tube, being a 6J6, contains two gates. (Note that the two center columns in each schematic are occupied by Gate Drivers. Note also that in each top row of toggles the convention is that 0 is signified by conduction of the left section, while in the bottom row the opposite is true.) As to the physical arrangement of the gates, the Red gate from column n to column n-1 is in column n, while the Black gate to column n from column n-1 is in column n-1, n signifying as before the first column in any Register Chassis. Furthermore, the Yellow gate between the toggles of column n-1 is physically located in column n. Thus in a complete forty stage Register, it is necessary to provide a Yellow gate for the 39th column, while half of the Yellow and Red gate tubes of column 0, and half of the Black gate tube of the 39th column are not actually used within the 40 Register stages, and hence are free for other uses: we shall see what advantages are taken of these circumstances when we examine the "end-around" circuits.

Now let us examine the actual uses of the gate tubes. In RI and RII the Red, Black, and Yellow gates are connected and used exactly as in the archetypal Shifting Register already described. The Green gates are, however, used to transmit information into $R^1$ and $R^2$ from other sources: into $R^1$ from the Digit Resolver, and into $R^2$ from $R^3$. In RIII the case is quite different, all gates being used for communication between the Register toggles and other parts of the machine, according to the following scheme:

(a) Red: into $R^3$ from the Discriminator in the Williams Memory.

(b) Black: into $R^3$ from $R_2$.

(c) Yellow: into $R_3$ from the Discriminator in the Williams Memory.

(d) Green: to Dispatch Counter from $R_3$.

We have seen how information is inserted in the Register toggles. Outputs are taken as follows:

(a) RI: from right-hand grids of $R_1$ toggles to Adder;

(b) RII: from right-hand grids of $R_2$ toggles to RIII Black gates;

(c) RIII: (i) from grids of $R^3$ toggles to Adder via the Complement gates;

(ii) from left-hand grids of $R^3$ toggles to RII Green gates;

(iii) from RIII Green gates to Dispatch Counter (already noted in the preceding paragraph).

RI has certain other circuits associated with it. One of these is an extra column to the left of the 0-th, in which the digit held in the 0-th can be

held in the case of a left shift, instead of being lost. The other is the "end-around" arrangement, which, in the case of a right shift, transfers the digit in the 39th column into the 0-th column of $R_2$.

The extra column is as shown in the diagram. The tube used to provide the Red gate into the lower toggle is already available in the 0-th column, while half the Yellow gate tube of that column is available as a Yellow gate for the new column.

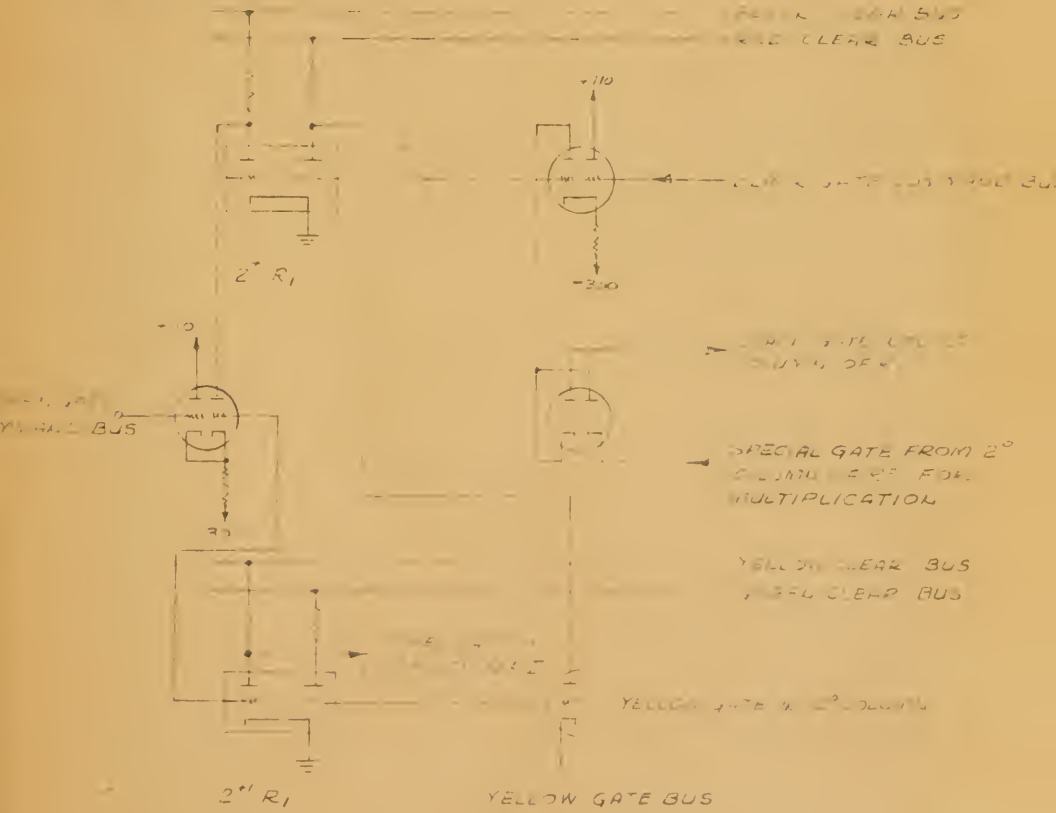


Fig. 10.

A Black gate is provided for right shifts. It will be noticed that a Green gate is also provided, which, unlike the other Green gates in RI, transmits from the lower to the upper toggle of the new column. The diode arrangement also permits the transmission of information from the 0-th column of $R^3$ to the corresponding column of $R_1$.

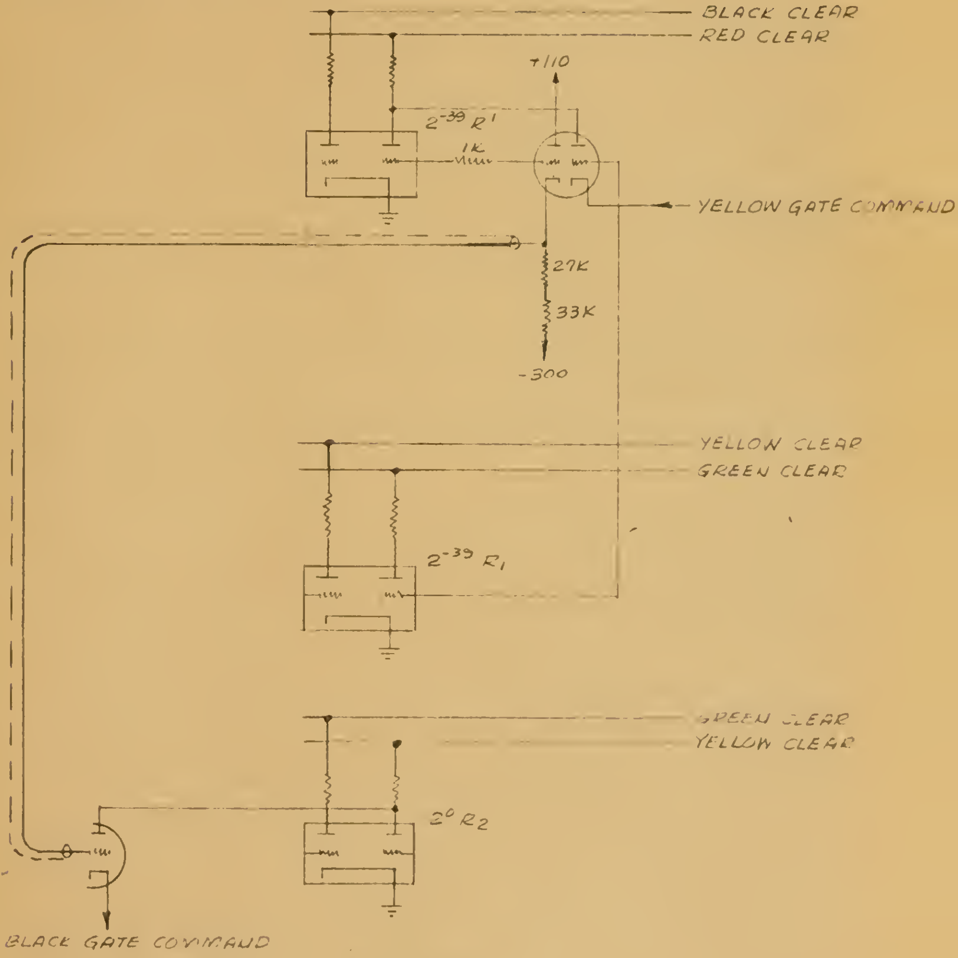


Fig. 11.

The transmission of the overflow from the 39th column of RI to the 0-th column of RII is simply taken care of by two additional tubes: One of these is a 2C51 mounted just beyond the extreme right end of RI: one section of this is used as a Yellow gate for the 39th column of RI, while the other is a cathode follower driven from one grid of the upper toggle of the 39th column, and driving a coaxial cable which runs back to the extreme left end of RII, as shown in Fig. 11. If right shifts are ordered in both RI and RII, the toggle in the 0-th position in R will have been cleared to 0 before the Black gate is opened. The opening of the Black gate will put into the 0-th stage of $R_2$ a 1 if a 1 was held in the upper toggle of the 39th stage of RI, otherwise there will be no change. Thus in any case the contents of $2^{-39}R^1$ is shifted into the 0-th stage of $R_2$. See Fig. 11.

The performance of the clearing operations in RI and RII is the function of the Clear Selector and Clear Driver Chassis: for each Register there is one Clear Selector Chassis and four Clear Driver Chassis, one for each of the types of clear operation used.

As the term indicates the Clear Selector Chassis determines which clear is to be performed. Fig. 12 shows half the tubes in the RI Clear Selector -- those which determine whether a Red or a Black clear is to be performed. This circuit consists of a 6J6 twin triode and two 6AL5 diodes. Note that the cathode of the 6J6 is either at +10v or at -10v, determined by the Logical Control Organ of the machine, while the grids are at either 0 or -40v. Thus as long as the cathode of the 6J6 is maintained at +10v, both sections of the tube will remain cut off, while the plate voltage will be maintained at +150v by the 6AL5 diode shown in the drawing just above the 6J6. This is in turn applied to the grid of the 6J6 Clear Driver cathode follower, whose

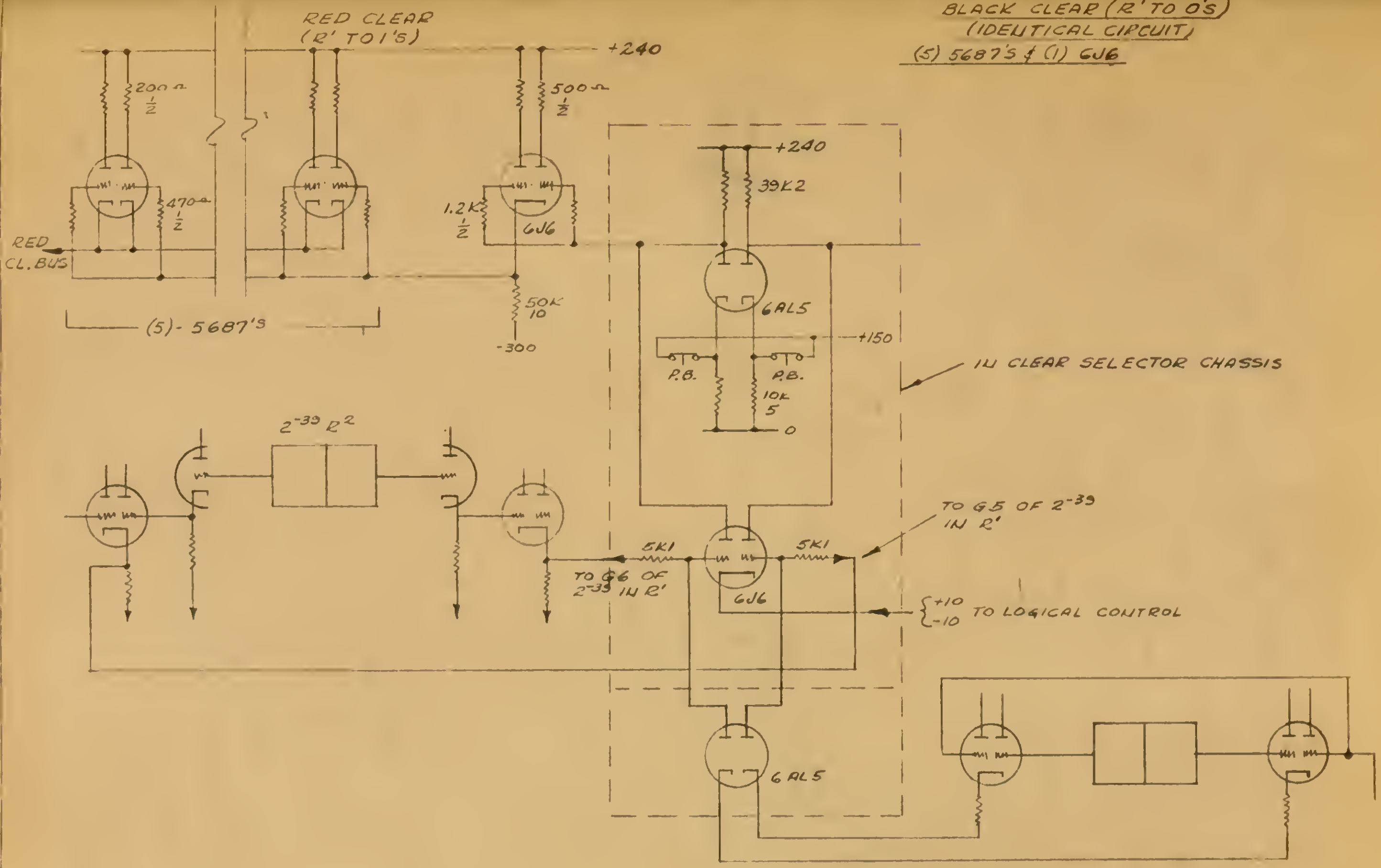
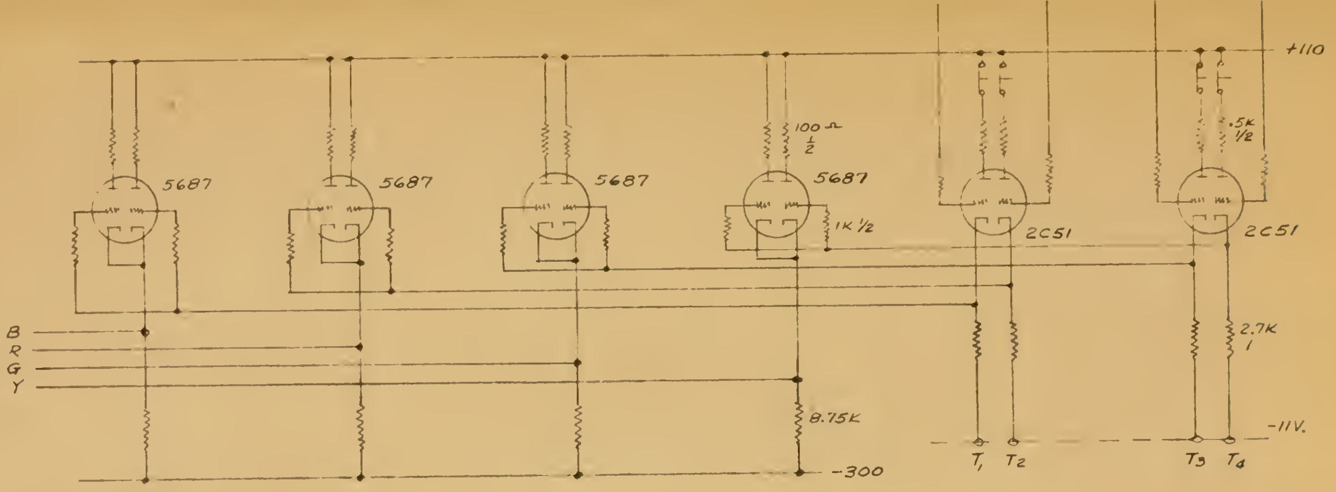

RED CLEAR
(R' TO 1'S)
+240
200 Ω
½
470 Ω
½
500 Ω
½
1.2K
½
6J6
RED
CL. BUS
(5)- 5687'S
50K
10
-300
BLACK CLEAR (R' TO 0'S)
(IDENTICAL CIRCUIT)
(5) 5687'S & (1) 6J6
+240
39K2
6AL5
+150
P.B.
P.B.
10K
5
0
IN CLEAR SELECTOR CHASSIS
$2^{-39}$ $R^2$
5K1
5K1
TO G6 OF
$2^{-39}$ IN R'
6J6
TO G5 OF $2^{-39}$
IN R'
+10
-10
TO LOGICAL CONTROL
6AL5

Figure 12

cathode in turn drives the grids of five 5687 tubes connected in parallel. The cathodes of these tubes are connected to the Red clear bus, which supplies plate voltage to the toggles of $R^1$. These tubes, therefore, again merely form a cathode follower of large current handling capacity. We, therefore, see that as long as the 6J6 in the Clear Selector remains in a cut off condition, the Red clear bus will be maintained at +150v.

Now let one of the grids of the 6J6 Clear Selector rise to 0v: to be explicit, the left-hand one, the right-hand one remaining at -40v. Nothing happens as long as the cathode is maintained at +10v, because the tube will remain cut off. Now let the cathode be switched to -10v. The left-hand side of the 6J6 will conduct, and the cathode will follow the left-hand grid to 0v, thus holding the right half in a cut off condition. Hence the right-hand plate of the 6J6 will remain at +150v, and the Black clear bus will be maintained at this voltage. The plate of the left half of the tube will, however, because of the plate current flowing through the 39,000 ohm resistor, fall to about 50v, which will cause the Red clear bus voltage to swing down to this value also. Reversing the voltages at the two grids of the 6J6 in the Clear Selector will clearly cause the Red clear bus to remain at +150v, while the Black clear bus will swing down to +50v. Another set of two 6AL5's and a 6J6 in the Clear Selector permit the choice of Green or Yellow clear operations. The toggles to be inspected in this case will be determined later; this is also the situation with regard to the Clear Selector for RII.

The circuits supplying the inputs to the grids of the 6J6 in the Clear Selector permit the inspection of the contents of two toggles -- one is that in the $2^{-39}$ position in $R_2$, the other is not yet determined. How the contents of these toggles are used to select the appropriate clearing operations



In RII Gate Chassis, $T_1$, $T_2$, $T_3$ are connected as shown, but $T_4$ is driven by the Yes-No signal from the Control: +10 = No, -10 = Yes.

Each gate bus drives 16 grids, 4 in each chassis.

Fig. 13.

will be shown in our description of the Logical Control of the machine.

In Fig. 13 is shown the schematic of the RI Gate Drivers and Gate Driver-Drivers. Each gate command is supplied by two cathode followers in cascade: the first, which we shall call the Gate Driver-Driver, is one section of a 2C51, while the driver itself consists of the two sections of a 5687 in parallel.

The Complement Gates permit either the number in $R_3$ or its one's complement to be read into the Adder. These are shown in the top row of DWG No. 1323. There is one 6J6 Complement Gate for each stage; every five of these have their plates driven by two 5687's connected as shown. Suppose the number in the toggle is a 0, the left grid being high, while the right is low. The left and right grids of the 6J6 gate tube will be then at about 0v and -40v, respectively. If the left grid of the 5687 is at +90v and the right one at -30v, then certainly the cathode voltage of the 6J6 will be 0v, signifying 0 to the Adder. If these grid voltages are interchanged, the 6J6 cathode voltage falls to a level of about -40v, signifying a 1 to the Adder. Thus, this arrangement permits us to transmit to the Adder either the contents of $R^3$ or its one's complement.

## ADDER AND THE DIGIT RESOLVER

The performance of the operation of addition is the function of the Adder and the Digit Resolver. Two numbers to be added are presented each as a set of forty voltages, 0v representing 0 and -40v representing 1, as inputs to the forty stages of the Adder. The Adder contains an analogue feature, in that voltages are added, in part, by the addition of currents in

a resistor. The output of each stage of the Adder is one of four possible voltages, corresponding to the four possible cases, in which the result of an addition is a 0 or a 1 with or without carry into the next column. The Digit Resolver is designed to discriminate between these four possible outputs, and to give as its output one of two different voltages, which are interpreted as 0 or a 1.

Each stage of the Adder has three inputs -- two representing digits of the number to be added, and one the carry from the stage which adds digits of the next lower column of the binary numbers to be added, and two outputs, one representing a carry to the next higher stage, the other being the one which the Digit Resolver must interpret as the appropriate digit of the sum.

The physical layout of the Adder closely resembles that of the Registers. The Adder thus consists of four chassis, each containing ten columns of four tubes each, one for each digit column of a forty binary digit number. The inputs are taken from $R_1$ (Resident digit) and from $R^3$ (Incident digit). In DWG No. 1334 will be found a schematic of one of the chassis, the other four being identical: only the first two and the last two columns of the chassis are shown in the drawing, as the rest are merely repetitions. It should be noticed that the left column of the extreme left chassis operates upon the lowest order digits of the numbers to be added -- that is, upon the digits in the column $2^{-39}$ -- and the order increases as we go to the right.

Consider the first two columns, which will be numbered n and n+1, in the Adder: reference should be made to the schematic, DWG No. 1334. For simplicity in reference, the tubes of column n will be labelled $T_{1,n}$, $T_{2,n}$, $T_{3,n}$, $T_{4,n}$, while those of column n+1 will be $T_{1,n+1}$, etc. The inputs are:

from $R_1$ (Resident digit) to grids 6 of $T_{2,n}$ and $T_{2,n+1}$; from $R^3$ (Incident digit) to cathodes 8 and 2 of $T_{3,n+1}$; carry from column n-1 to grid 6 of $T_{4,n}$, and carry from the n-th column to grid 6 of $T_{4,n+1}$. Thus tubes $T_{1,n}$, $T_{2,n}$, $T_{4,n}$, and the left halves of $T_{3,n}$ and $T_{3,n+1}$ perform the addition in the n-th column while $T_{1,n+1}$, $T_{2,n+1}$, $T_{4,n+1}$ and the right halves of $T_{3,n}$ and $T_{3,n+1}$ perform that in the n+1-th column. The following names for the tubes are descriptive of their functions: $T_{1,n}$ - "carry gate"; $T_{2,n}$ - "resident digit gate"; $T_{3,n}$ - "summing resistor driver"; $T_{3,n+1}$ - "incident digit gate"; $T_{4,n}$ - "summing resistor driver driver".

In the interests of clarity we will consider the possible cases, and observe the action of the circuit in each case. These cases are:

| | (1) | (2) | (3) | (4) | (5) | (6) | (7) | (8) |
|---|---|---|---|---|---|---|---|---|
| Resident digit | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Incident digit | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Carry from next lower stage | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Sum | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| Carry to next stage | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

Thus there are seven possible inputs, but only four possible outputs.

First consider case (1). Here the Incident and Resident digits (i.e., inputs to cathode 8 of $T_{3,n+1}$ and to grid 6 of $T_{2,n}$) are both 0v, and we can consider the carry digit connection as cut -- it will appear as we go on that this is correct, as no current flows through this wire except when there is a carry from the preceding column. Under these conditions the cathode of the Summing Resistor Driver Driver is slightly above +211v. Hence the cathode of the left half of the Summing Resistor Driver is slightly higher than this,

so that the voltage at the grid of the Summing Resistor Driver, which is directly connected to this cathode is 215v. Furthermore, the left half of the Resident digit gate will be in a conducting stage, so that by cathode follower action the cathode will be nominally at the grid potential, or 0v, and the right half will, therefore, be cut off, since its grid is maintained at -9v. The left half of the Incident digit gate will also be cut off, since its grid is at -9v and its cathode at 0v. Thus no current will be drawn through the Summing Resistor (connected between the Summing Point and the cathode of the Summing Resistor Driver) by either of these gate tubes. The cathode of the carry gate will follow the more positive grid and, therefore, rise to 215v, so that the left half of this tube will be in a conducting state and the right half cut off. Hence the voltage at point S will be +215v, as no current flows through the Summing Resistor, and no current flows through the carry connection to the next stage, showing the correctness of our original assumption.

In cases (3) and (5), we still consider the carry into the n-th stage as disconnected. In case (2) the Incident digit input drops to -40v, which permits conduction by the Incident digit gate; the cathode of this tube will, of course, only drop to slightly above -9v. Thus the plate current drawn will be very nearly 165/32 ma = 5.15 ma, which flowing through the Summing Resistor will cause a drop in voltage across this resistor of very slightly more than 54 volts. As the right half of the Resident digit gate is cut off, the output voltage to the Digit Resolver is +161v. In case (4), the Incident digit gate is cut off, but the right half of the Resident digit gate is now conducting; again the plate current of 165/32 ma causes a drop of 54 volts in the Summing Resistor, so that the output voltage is again +161v. In both cases (2) and (4) we see that the left grid (6) of the carry gate tube ($T_{1,n}$)

being at +157v, the cathode of this tube will be slightly more positive, and the right half will remain cut off. Thus we have shown that the condition of "no carry" implies that no current will flow through the "carry" connection to the next stage, which is the assumption that has been used all along in the analysis.

It has now been shown that if the Incident or Resident digit is a 1, the circuit will cause the corresponding gate to draw 5.15 ma through the Summing Resistor. Hence in case (7) a total of 10.3 ma will flow through this resistor, and the output voltage to the Digit Resolver will drop to +107v. Thus grid 6 of the carry gate will drop below grid 5, which means that the right half section of this tube will now conduct, the cathode will rise to slightly more than +136v, the left section will be cut off and the right section will draw very nearly 436/90 = 4.85 ma. This state, which indicates a carry into the next stage, causes the grid of $T_{4,n+1}$ to drop to approximately +124v.

Now consider case (2). Here grid 6 of the Summing Resistor Driver Driver ($T_{4,n}$) is held at +124v; the diode-connected right half has its plate maintained at +161v; hence this section will conduct, and the cathode voltage will rise to slightly below +161v. This will, therefore, fix the voltage of the cathode of the Summing Resistor Driver. (At slightly below this level; there is, however, a slight rise in voltage from grid to cathode of the Summing Resistor Driver, so that the voltage at this point turns out to be very close to +161v.) Since no current is drawn through the Summing Resistor, the Summing Point voltage ($V_s$) is +161v. This is also sufficient to raise the cathode of the carry gate to +161v, and to keep the right half of this tube in a non-conducting state.

The remaining cases can now be discussed. In cases (4) and (6) the action of the carry from the preceding stage is to lower the cathode voltage of the Summing Resistor Driver to +161v, while the effect of the Incident or Resident one, as the case may be, is to cause a voltage drop of 54 volts across the Summing Resistor. Thus the output $V_s$ = 161 - 54 = 107v. Hence the right half of the carry gate will conduct, and so a carry will be indicated to the next stage.

Only case (8) now remains. Here the Summing Resistor Driver cathode voltage is +161v because of the carry from the preceding stage, while the current drawn by the Incident and Resident gates through the Summing Resistor causes a drop of 108 volts across the Summing Resistor, so that $V_s$ = 161 - 108 = 53v.

To sum up, there are four possible results to the addition in the n-th column: the table gives these, and the corresponding $V_s$.

| Sum | Carry | $V_s$ | $V_s$ (average measured values) |
|---|---|---|---|
| 0 | 0 | 215 volts | 215.3 volts |
| 1 | 0 | 161 volts | 161.0 volts |
| 0 | 1 | 108 volts | 108.4 volts |
| 1 | 1 | 53 volts | 55.9 volts |

It is now necessary to provide a means by which these output voltages are interpreted; the result of this interpretation must be that $V_s$ = 215 or 108v ultimately set a toggle in the 0 position, while $V_s$ = 161 or 53v set it in the 1 position. We need not worry about carries, as we have seen that these are all automatically taken care of in the Adder. The task of interpretation is assigned to the Digit Resolver, which will now be described.

Physically the Digit Resolver consists of four chassis similar to those used in the Adder and located directly above them. Each column of tubes in the Digit Resolver is assigned to interpret the output of one column of tubes in the Adder. Thus the columns of tubes in the Digit Resolver are independent of each other, accepting a single input ($V_s$) from the Adder, and giving a single output to $R^1$. A schematic of a single column of tubes in the Digit Resolver is shown in DWG No. C-3-1107. For convenience these will be labelled $T_1$, ..., $T_4$ in order from the top downward.

We shall consider in order the four possible cases. First let $V_s$ = +215v, which being applied to grid 5 of $T_3$ causes the cathode to rise slightly higher, thus cutting off the right section of $T_3$ and the left section of $T_4$. Furthermore, the cathode of $T_1$ is raised above +215v, cutting off the right section of that tube. Now consider $T_2$. If the plate and grid of the left section were disconnected, grid 3 would assume a potential of approximately +163v. Actually, of course, grid current flows, so that the grid is only slightly positive with respect to the cathode. Plate current amounts to about 4 ma which is more than sufficient to hold grid 7 below cut off. Thus the output voltage is determined by the voltage divider consisting of the 43.16K, 128.7K, and 188.1K resistors to be +32v.

In the second case, $V_s$ = +161v. This is still sufficient to hold the right section of $T_3$ in a non-conducting state, but not enough to do the same for the left section of $T_4$, which accordingly conducts, while the right section is cut off. Again the voltage of grid 6 of $T_1$ (+161v) is more than enough to assure that the right section is cut off. As the left section of $T_4$ draws approximately 488/139 ≑ 3.5 ma, the voltage of grid 3 of $T_2$ falls to about +86v, and the left section of the tube is, therefore, cut

off. The voltage of grid 7 of $T_2$ would now become +116v but for the flow of grid current, which holds it down to but little above +82v (the voltage of cathode 8), and the output voltage falls to about -58v.

In the third case, $V_s$ = +108v. Again the left sections of $T_3$ and $T_4$ conduct, while the right sections are cut off. Hence as in the second case the grid voltage of the left section of $T_2$ is well below cut off. However, the voltage of grid 6 of $T_1$ is now but slightly above +108v, while that of grid 5 is +136v: the cathode follows the more positive grid, the left section is cut off, and the right section draws a plate current of very nearly 4 ma. As in the first case, this holds the voltage of grid 7 of $T_2$ safely below cut off, and again the output voltage is approximately +32v.

Finally, in the fourth case $V_s$ = +56v ( to use the average measured value). Hence in $T_3$ the right section conducts, while the left section is cut off. The right section of $T_4$ and the left section of $T_1$ are cut off, while the other sections conduct, and consequently, as in the third case, both sections of $T_2$ are cut off. Now, however, the plate current drawn by the right section of $T_2$ through the 43.16K resistor causes the output voltage to fall to about -48v.

To sum up, the Digit Resolver output is +32v in both cases where the sum digit is 0, while it is far negative in both cases where the sum digit is 1. These voltages are actually considerably larger than needed to operate the RI Green gates. Hence a diode "bumper" is provided at the output of each stage: the circuit is shown in DWG No. 1288. In stages $2^0$ to $2^{-35}$, the diode cathodes are returned to ground, while in the remaining stages they are returned to ground except during the read-in of information from the Input. Thus during ordinary operation, the Digit Resolver output never swings above 0v, while the negative excursion is not limited.

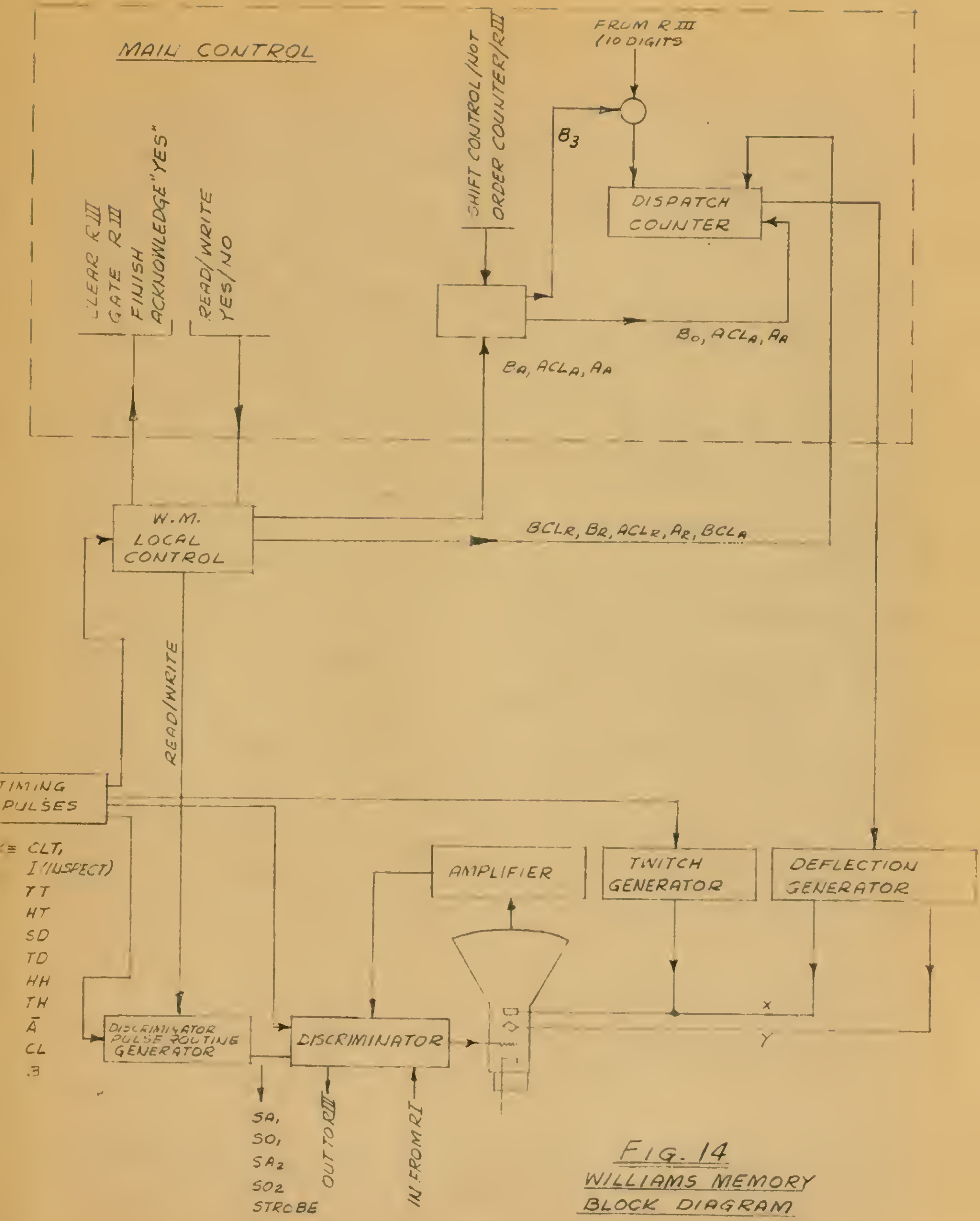


FIG. 14
WILLIAMS MEMORY
BLOCK DIAGRAM

# III. THE WILLIAMS MEMORY

## WILLIAMS MEMORY BLOCK DIAGRAM

There is no need to enter into a discussion of the physical processes that occur in a cathode ray tube used as a storage device in the way first proposed by F. C. Williams, as this has been done elsewhere. We will describe how cathode ray tubes are incorporated in electronic circuits in order to produce a complete memory organ. In the interests of clarity, we will first discuss the functions which the circuits are required to perform: from this a block diagram can be constructed. When the main features of the memory organ have been thus presented, it will be time to describe in detail the actual circuits, and to show how the required functions are performed.

The memory organ of the present machine is of parallel type, holding 1024 bits per tube in a square array, so that 40 tubes store 1024 forty binary digit numbers, one binary digit of each number being held in each tube. A slight modification of the "dot-dash" scheme of storing 0's and 1's is used, in that a "dash" here signifies two "dots" written so closely together that the charge distribution produced by the writing of the first of the pair is considerably modified by that produced by writing the second. Thus we may suppose that the charge distributions are qualitatively as follows:

Dot (0)

Double Dot or Dash (1)

Fig. 15.

This picture needs to be kept in mind while we consider the writing process.

To write a dot, we must first generate the deflection voltages which guarantee that the beam will be directed to the desired location and then turn on the electron beam for a short time. In writing a dash, we must do more: first a dot must be written, then, after the electron beam has been turned off, the beam position must be moved slightly to one side ("twitched"), then the electron beam must be turned on again for a short time. Thus we have for each memory location two positions: One for the first peak of charge, a second for the second peak of charge; these will be referred to for convenience as the A and B positions.

In either writing new information or in regenerating what already exists, it is clear that logically we need be able to make only a choice between the two states of charge that are used to represent 1's and 0's, and hence between two routines for turning on the electron beam. However, the physical processes of writing a dash where a dot exists, or a dot where a dash exists, are certainly somewhat different from those of merely "restoring" a dot or a dash. Consider the writing of a dot on a dot: we merely have to build up the charge in the A position to its equilibrium position. On the other hand, if a dash already exists and we wish to write a dot over it, it is clearly desirable to leave the beam on in the A position for a longer time, so that more secondary electrons will be permitted to return to the screen to nullify the concentration of positive charge in the B position.

If a dash is to be written where a dash already exists, it is clearly sufficient to turn on the beam in the A position only very briefly, while in the B position it must stay on long enough to bring the charge up to the equilibrium value. On the other hand, in writing a dash over a dot, it is

desirable to leave the beam on in the B position somewhat longer, in order that more secondary electrons will be available to return to the screen and nullify in part the accumulation of positive charge in the A position. Thus we are led to distinguish four possible routines:

(1) Write a dot where a dot exists ("normal dot") (TT)
(2) Write a dot where a dash exists ("superdot") (HT)
(3) Write a dash where a dash exists ("normal dash") (HH)
(4) Write a dash where a dot exists ("superdash") (TH)

In the brief designations of these four processes (TT, etc.), the letters T and H are the last letters of dot and dash, the first position signifies the existing state before the writing process, while the second signifies the state to be created. In all cases the beam is turned on in position A in order to sense what information is stored in the location in question: this is obviously necessary in the reading or the regeneration process, while in the writing process, it is necessary to compare this information with that which is to be written, and thus to select which of the four routines TT, HT, HH, TH is appropriate. The following timing diagram for the turning on of the electron beam is useful.

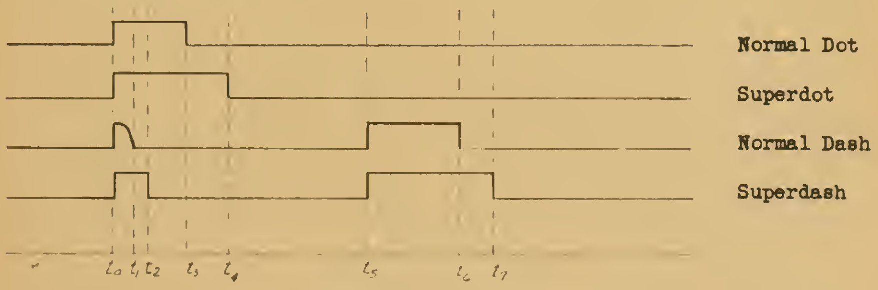


Fig. 16.

In all cases the electron beam is turned on at $t_0$, while between $t_4$ and $t_5$, a period during which in all cases the beam is turned off, the "twitch" takes place; thus in $t_0t_4$ the beam is directed toward the A position, while in the $t_5t_7$ it is inthe B position. We note that in the Normal Dash routine the beam is on in the A position for a shorter time than it is in the Superdash routine: here an automatic turn-off of the beam occurs, which will be explained when we describe the operation of the Discriminator circuitry.

We have seen what beam-turn-on routines are needed for performing the read-regenerate and the write functions. To carry out these routines, properly timed sequences of pulses are needed in each case. Hence it is necessary to provide not only these pulses, but also means of selecting the required sequence, means of "reading" what is stored in any given memory location, and means of deflecting the cathode ray tube beam to the desired memory location. Furthermore, since the contents of the memory must be periodically regenerated, it is clear that a fundamental repetition rate must be provided.

In the following discussion we shall illustrate, with reference to the block diagram, how the functions outlined above are accomplished. It is simplest to start with the cathode ray tube-amplifier-discriminator loop. It should be noted that each of the forty CRT's in the memory organ has its own output Amplifier and Discriminator; all the equipment represented by other blocks in the diagram is common to the forty CRT's. At the beginning of each read-regenerate or write cycle the Discriminator turns on the electron beam in the CRT by raising the potential of the control grid. The Amplifier merely raises the CRT output signal to the required level, which calls for a gain of about $2 \times 10^4$, its output being used to set to 0 or 1 a toggle in the Discriminator, which has previously been cleared to 0. The Discriminator inputs

are, in addition to that from the Amplifier: (1) pulses to clear the toggle and initiate the beam turn on routine -- these are the same no matter what routine is performed; (2) four pulse trains $SO_1$, $SA_1$, $SO_2$, $SA_2$ which differ according as reading, regenerating, or writing is required; (3) the digit to be written from $R_1$, this being via a gate which is enabled only when writing is called for. In addition to the beam-turn-on output, there is one from the Discriminator toggle to RIII, which is via a gate enabled only when reading is required.

A block labelled "Timing Pulses" appears in the diagram. Physically this contains a "Memory Clock" which provides the basic repetition rate, and nine "Pulsers" which generate pulses beginning at various times in the cycle: these pulses are of different lengths as required, and each is immediately followed by a standard "termination" pulse. These are: Inspect, TT, HT, Twitch Delay (TD), HH, TH, and three others; $\bar{A}$, Cl, and B, which are needed to step the Dispatch Counter in the Main Control. Termination pulses are designated by a small "t" subscript: as $SD_t$, etc. The time sequence is illustrated in Fig. 17, where the "termination" pulses are omitted. The clock pulse is also used to clear the Discriminator toggle to 0, and so is usually designated by the abbreviation "Cl $T_1$".

It has been remarked that it is necessary to provide the Discriminator with four trains of pulses, $SO_1$, $SA_1$, $SO_2$, $SA_2$ to enable it to carry out the read-regenerate process, and a different set of four trains to carry out the write process. These trains are formed from the timing pulses just discussed in the block labelled "Discriminator Pulse Routine Generator"; it will be noticed that there is an input to this block labelled "Read/Write": this signal determines which set of pulse trains $SO_1$, ..., $SA_2$ will be transmitted

to the Discriminator.

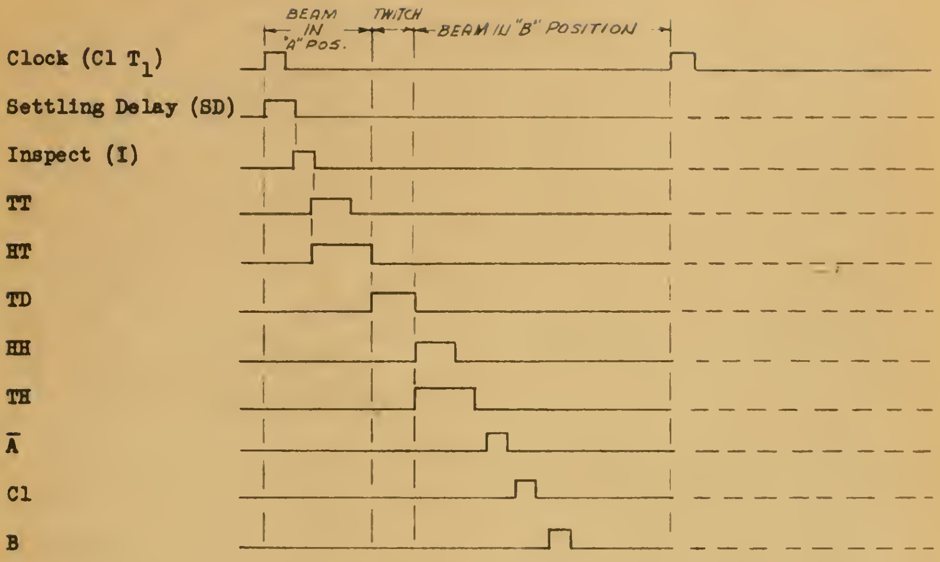


Fig. 17.

The Read/Write input to the Discriminator Pulse Routine Generator comes from the block labelled "Local Control". Here signals are received from the Main Control (not, of course, a part of the Memory), and from the Timing Pulse Generator. The signals from Main Control signify: (1) "Yes/No" - the Memory is to be used or not; (2) "Read/Write" - a read-regenerate or a write routine is called for. Local Control transmits the Read/Write signal to the Discriminator Pulse Routine, and also actuates the electronic switch which determines whether the address standing in the Dispatch Counter or that standing in $R_3$ is to be transmitted to the Deflection Generator. Local Control also transmits back to Main Control the following signals: Acknowledge "Yes", Clear RIII, Gate RIII, Finish, whose significance will be made clear when we undertake

the detailed description of the Local Control.

Finally, the Deflection Generator merely receives as inputs the coordinates of the Memory location to which the CRT electron beam is to be directed and generates the appropriate deflection potentials. The "twitch" generator's function is obvious: it is actually part of the Deflection Generator, but its action is initiated by the HT (superdot) termination pulse.

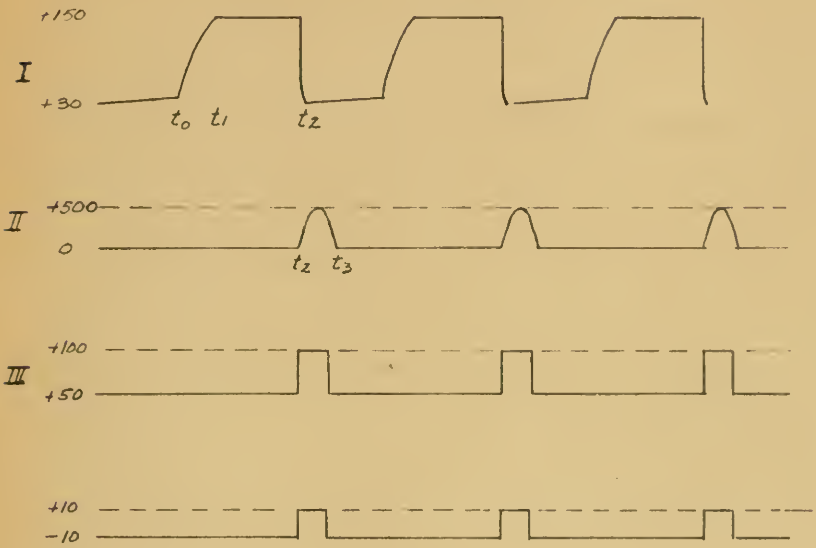
## MEMORY CLOCK

The necessity of periodically regenerating the information stored in the Williams Memory makes it necessary to provide a timing device. In the present machine, this is called the "Memory Clock".

As there is nothing in the operation of the Memory that requires the maintenance of a very precise repetition rate, and as it is desired to permit the rate to be varied over a rather wide range (from 4kc to 143kc in the present model), for convenience in testing it is entirely feasible to use a multivibrator as the fundamental rate-determining circuit. The output of the multivibrator is used merely to ring a parallel LC circuit, the natural period of which determines the pulse duration.

The Memory Clock schematic is given in DWG No. 1217. The multivibrator appears at the left of the drawing, (tube B (a 6J6) and its associated components). The diode A is added to sharpen the plate voltage recovery. The plate voltage of the conducting half of the 6J6 falls to about 30v; when this section of the tube is cut off, its plate voltage begins to rise exponentially toward 300v; and hence is rising quite steeply when it reaches 150v, where it is stopped by the diode. Hence, the multivibrator output resembles waveform I in Fig. 18. The fall in plate voltage is quite abrupt; this sharp

trailing edge is the important feature of the output as it affects the rest of the circuit.



($t_2t_3$ is approximately .9 microsecond; the time between pulses depends upon the p.r.r. chosen)

Fig. 18.

To insure against spurious triggering of the multivibrator by noise, the whole Memory Clock is housed in a metal box, and low pass filters are inserted in the leads by which power is brought in, as shown in the schematic. The dually controlled 500k variable resistors and the condensor switching arrangement make it possible to vary the repetition rate of the multivibrator from 4kcps to 143kcps. The present p.r.r. is 25kcps: this will be raised

considerably in the future.

The output from the multivibrator is taken from the plate of the right-hand section, and applied to grid of the left-hand section of tube D (a 6J6). The coupling network time constant is .001 sec., which is sufficiently larger than the longest period available so that no serious distortion results, while the left-hand half of the diode C merely clamps the top of waveform I to ground. Thus the input to tube D is again waveform I, but now the swing is from 0v to -120v.

Now consider tube D. Its right-hand grid is maintained at -10v, so that during that part of the cycle when the left-hand grid is at ground potential, the left half is in a conducting state, drawing plate current through the 2.4 mh inductance; the cathode will be slightly above ground potential and the right half consequently cut off. At time $t_2$, the left grid suddenly falls to about -120v, so that the left half will be cut off, and the current transferred to the right half.

Thus the initial conditions for the circuit formed by the inductance in parallel with its distributed capacity are: current flowing in the coil, and a slight charge in the capacitance. The parallel LC circuit will, therefore, begin to oscillate. The voltage across the coil will start at close to 0 (actually a volt or two, due to the non-0 resistance of the coil), and will so swing that the voltage of the end of the coil not attached to the +100v bus will go positive with respect to +100v; this excursion of amplitude approximately 50 volts, will, of course, be sinusoidal, at the natural frequency of the LC circuit (which is very close to 5 mcps). When, however, the first half period has ended, and the end of the coil not attached to the bus begins to swing negative with respect to the bus, the right half of diode C

will begin to conduct: this, together with the 4.7k resistor critically damps the LC circuit, so that at each fall of voltage at the right-hand plate of the multivibrator, a single positive half sine wave is transmitted to the grids of tube F. The d.c. level from which this swing starts is clamped to 0v by the left section of diode E. The signal applied to the grids of tube F is, therefore, as shown in waveform II. The internal $t_2t_3$ is very nearly one microsecond, and this is clearly independent of the repetition rate of the multivibrator.

Tubes F and G are both 6J6's each being so connected that it acts as a single tube. The grids of G are maintained at +10v, so that, as long as the grids of F are held at ground potential, the cathodes of both tubes, which are connected together, are held at slightly above +10v, with the consequence that F is cut off. Now in the interval $t_2t_3$, during which the grids of F are driven to approximately +50v, tube F is caused to conduct so that its cathode follows the grid so high that G is in turn cut off: this causes the plate voltage of G to rise sharply from about 50v to 100v; of course, it will fall sharply by a like amount when current switches from G back to F again shortly before $t_3$. Thus the plate voltage of tube G is as shown in waveform III.

We now have to consider only the output cathode follower, tube H. With the left-hand grid held at -10v, and the right at -25v, a condition which persists except in the intervals $t_2t_3$, the left half will conduct, the right half will remain cut off, and the cathode potential will remain at very little above -10v -- which is the output voltage from the Memory Clock in these intervals. When now in intervals $t_2t_3$ a 50v pulse is emitted by tube G, the voltage of the right-hand grid of G will rise to +10v, where it will be caught by the right half of diode E; consequently, the cathode of H will rise to

very slightly above +10v during time intervals $t_2t_3$, which gives us the output waveform IV.

## WILLIAMS TUBE PULSERS

The operation of the Williams Memory requires the availability of a number of pulses occurring at definite times in the cycle of the Memory Clock (see Fig. 17). The circuits used to provide these are called "Pulsers". They are all designed to accept as inputs pulses of essentially rectangular shape, rising from -10 to +10v, and of duration .5 µs or greater. The pulser output consists of two pulses. The first is one whose length may be varied; the leading edge of this pulse occurs at the same time as that of the input pulse. The second is in all cases of fixed duration -- approximately .5 µs -- with its leading edge synchronized with the trailing edge of the first pulse. The second pulse output is of about half the duration and of the same amplitude as that of the Memory Clock, and can be (and is) used as an input trigger to other pulsers. Both time durations are established as one half the period of a parallel LC circuit. In the case of the first pulse, variation of the values of inductance and capacitance permit variation of pulse duration over a fairly wide range. A table is given in DWG No. 1216 which shows the ranges of pulse duration available in the pulsers of the present machine.

Let us now consider the operation of the circuit (see DWG No. 1216). Between pulses the right-hand grid of tube A is held at -20v and the left-hand grid at -10v. Under these circumstances, the cathode of A is slightly above -10v, the right half of A is cut off, and in tube B, the left- and right-hand grids of which are at -10v and ground, respectively, only the right half is in a conducting state, plate current of approximately 4.2 ma

being drawn through the 1 mh inductance. We assume that no transient oscillation is present in either LC circuit: the fact that each LC circuit has connected across it a diode (consisting of the cathode and one grid of tube C) and resistance chosen at the critical damping value of the circuit assures us that no transient will persist essentially beyond one period. Thus both plates of B are very nearly at +150v (the left grid will be at this voltage, while the right one will be very slightly below because of the non-0 resistance of the 1 mh inductance). Thus the cathode and both grids of tube C are at +150v, so that both sections are in a conducting state; the plate potentials turn out to be about +225v. Clearly diodes D and E are now conducting, while only the right half of tube F is conducting, the cathode, therefore, being slightly above -10v.

With the arrival of the input pulse at the left grid of tube A, the cathode will follow the grid to slightly above this voltage: we note that this is also automatically the leading edge of the "Pulse Out", which is, therefore, not delayed with respect to the input pulse.

The left-hand grid of tube B is now driven to slightly above +10v, and the cathode follows it, thus cutting off the right-hand section. This abrupt switch, of course, sets up transient oscillations in the parallel LC circuits in the plate leads of tube B. The right-hand plate swings positive with respect to +150v. Thus the left-hand grid of tube C becomes positive with respect to the cathode; and grid current flows through the 2.2K resistor in series with the grid: the value of this resistor is chosen so as to assure that the parallel RLC circuit consisting of the inductance and capacitance, the grid-to-cathode resistance of the left section of C, and the 2.2K resistor is critically damped. Of course, the plate current of the left section of C

is increased somewhat and the plate voltage decreased; this change is transmitted to the left grid of tube F, which has already been shown to be below cut-off. Hence this transient has no effect on the output of the Pulser. On the other hand, the transient set up in the plate circuit of the left section of B is such that the plate swings negative with respect to +150v: the exact amount of this swing, of course, depends on the square root of L/C; for all the values used it is never less than about 28v. The right section of C cuts off when the grid is about six volts below the cathode, a level which is reached in at the most 7% of the half period of the LC circuit. The plate voltage is not, however, permitted to rise all the way to +300v; it is "caught" at +260v by the left section of diode D, a level which will obviously be reached considerably before the grid voltage reaches cut-off, so that the rise from +225 to +260v is accomplished in a little over 3% of the half-period of the LC circuit: at the end of the half-period, of course, a fall of like amount takes place. Thus a pulse of about 35v amplitude is created at the right-hand plate of C. The right-hand plate of the 30 $\mu\mu f$ condenser is maintained at -20v before the pulse begins, so that since the cathode of diode E is held at +10v, at this point a pulse rising from -20 to +10v appears: these levels are accurately defined, and it is apparent that the exact magnitude of the pulse at the right plate of C is unimportant provided it exceeds 30v. A similar remark applies to the magnitude of the negative swing of the right grid of C: it needs only to be sufficient to raise the plate voltage to +260v in a time short compared to the half-period of the LC circuit. The pulse produced is applied to the right-hand grid of tube A, which rises to +10v. Thus though the input pulse to the left grid of A shortly drops from +10 to -10v, the cathode is held at slightly

above +10v for a time determined by the half period of the LC circuit.

At the end of the negative swing of the right-hand grid of C, the voltage of the right-hand grid of A falls again to -20v; the cathode, however, is "caught" at -10: this fall marks the end of the "Pulse Out." This fall also causes a switch in current in tube B: the right-hand half once more is caused to conduct, and the left is cut off. We must once more examine the behavior of the LC circuits in the plate leads.

It is now time for the second half cycle of the oscillation of the circuit in the left plate lead. However, when the lower end of this starts to go positive with respect to the upper end, the right section of C begins to draw plate current, and its grid to cathode resistance, in addition to the 2.7K resistor, critically damps the oscillation. The drop of the plate voltage of this section below +225v drives the right-hand grid of A below -20v, but this clearly has no effect upon the cathode voltage of A, and hence the "Pulse Out" voltage, which remains at slightly above -10v.

However, the 1 mh inductance -- 20 $\mu\mu$f condenser combination now produces a transient: the end connected to the right-hand plate of B swings negative with respect to +150v through a half period of a sine wave of about 28v amplitude. This drives the left half of C below cut-off; the plate voltage begins to rise toward +300v, but is caught at +260v by the left section of diode D, and we get a pulse of approximately 35v amplitude lasting for nearly .5 $\mu$s at this point. Note that in determining the period of oscillation it is necessary to take into account, in addition to the 20 $\mu\mu$f condenser, any distributed capacity that is present -- this is of sufficient magnitude to make the resonant frequency close to 1 mcps. Diode E limits the rise of grid voltage of the left section of F, so that this point rises from

-20v to +10v during the pulse, and hence the cathode rises from slightly above -10v to slightly above +10v for very nearly .5 μs. This is the "Pulse End" pulse: as we said before, its leading edge is determined by the termination of the Pulse Out pulse. As the 1 mc oscillation attempts to enter its second half cycle, the left half of C draws grid current, and critical damping again ensues. Thus the circuit is returned to its quiescent state, awaiting the arrival of the next input pulse.

There are ten pulsers of the kind just described. One of these, the "Settling Delay" pulser, is triggered by the Clock pulses; its pulse output is not used, but its termination pulse triggers the Inspect, TT and HT pulses. The termination of the HT pulser triggers the TD pulser, and its termination pulse triggers both the TH and HH pulsers. The TH termination pulse triggers the $\bar{A}$ pulses, its termination pulse the C1 pulser, and finally its termination pulse the B pulser. A pulse called the "Strobe" is used in the Discriminator: it is an inverted and slightly amplified version of I, dropping from 0 to about -25v for the duration of I. It is generated by a circuit located in the same chassis that contains the Local Control and the Pulse Routine Generator and will be described with them.

Fig. 19 shows the actual waveforms observed, together with the timing actually used in the computer. We will see later how various of these pulses are combined to give the Discriminator Pulse Routine voltages used in the Discriminator. We also note that the I pulse is not used directly, but is first passed through an amplifier and d.c. restorer to produce the negative-going pulse actually used in the Discriminator. The actual voltage levels employed are shown in Fig. 19: these are very close to the "nominal" values of -10v and +10v which we used in the discussion of the pulser circuit:

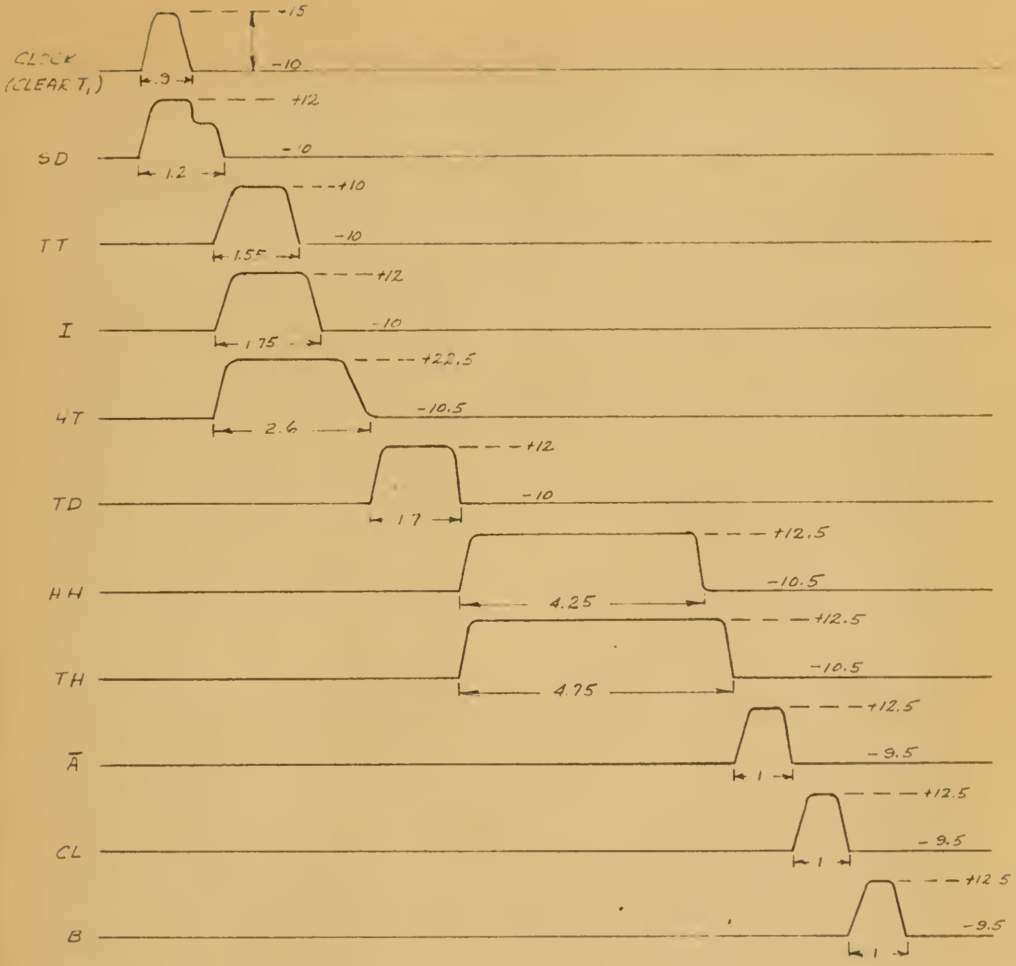


Figure 19
(PULSE DURATIONS GIVEN IN MICROSECONDS)

moderate deviations from the nominal values have no effect on the operation of the circuits to which the pulser outputs are applied.

The termination pulses are not shown. However, these all rise at the

termination of each pulse and last for approximately .5 µs. They are designated by the letter that describes the pulse at whose termination they rise with a small "t" subscript, as for example $I_t$, $TD_t$, etc.

## THE WILLIAMS TUBE OUTPUT AMPLIFIER

The current that flows to or from ground to the cathode ray tube pickup screen during a reading operation is very feeble. A resistor being inserted between these points, the resulting voltage must be amplified to bring the output up to the desired voltage level. Thus each cathode ray tube in the Williams Memory is provided with an amplifier, the schematic of which appears in DWG No. 1142. In this drawing is shown also the physical structure of the amplifier, which will be seen to be of annular form: it is mounted within the shield that encloses the cathode ray tube, directly in front of the tube, which minimizes the length of the lead from the pickup screen to the grid of the first tube of the amplifier.

The value of R-5 was chosen as 100,000 ohms, which means that the maximum amplitude of input voltages are approximately .25 mv and 1 mv when a 0 or a 1, respectively, is read. A gain of 20,000 provides output signals of maximum amplitude 5 and 20v, respectively, which are ample for the purpose for which they are used in the Discriminator. Using three stages of amplification, with 6AK5 tubes, and assuming $g_m$ = 4000 µmhos, requires a load resistor of 6.8K for a gain of 27.2 per stage, very nearly 20,000 overall.

It was desired to hold to a low value any 60 cycle hum due to cathode leakage and modulation of the electron stream. Given the chosen value of grid-leak resistance, the value of 1000 µµf for C-4 is chosen to guarantee

that the gain at 60 cps is less than unity. As the tubes are to be operated at not over half the rated plate and screen dissipation, the decoupling resistor R-2 and the screen grid resistor R-1 were chosen so that with 0 input voltage and 2.5v bias developed across R-4 neither the screen nor the plate voltage exceeds 120v.

The remaining elements are the peaking inductance L-1, and the three condensers C-1, C-2, C-3. The value of C-2 is as large as can be conveniently incorporated in the assembly; that of C-3 is not critical since the low-frequency response of the amplifier is not particularly important; C-3 is sufficiently large that any serious reduction in gain due to degeneration is avoided for the middle range of the amplifier response and beyond. C-1 again is not critical.

The measured gain characteristic of the amplifier has half power frequencies at very nearly 6 kcps and 300 kcps. One other characteristic of the amplifier response is the rise time, which here turns out to be approximately .3 μsec.

## THE DISCRIMINATOR

The signals obtained from the cathode ray tubes, after having been inverted and amplified by the three stage output amplifier are as follows:

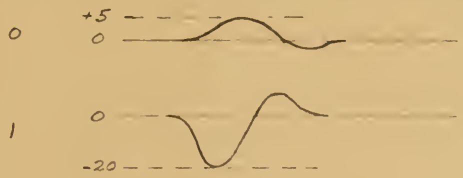


Fig. 20.

The Discriminator distinguishes between these two: it contains a toggle which is set by the amplifier output to the state corresponding to the bit of information read. The Discriminator is furthermore supplied with four trains of pulses from the block in Fig. 14 labelled "Discriminator Pulse Routine Generator", which are of one configuration if reading or regenerating is called for, but of a second configuration if new information is to be written over that presently in existence. If reading or regeneration takes place, the Discriminator causes the electron beam of the cathode ray tube to be turned on the required time (Normal Dot or Normal Dash) to restore the existing state of charge, while if writing is to be accomplished, the circuitry compares the existing bit of information with that which is to replace it, and turns on the electron beam in the Normal Dot or Normal Dash routine if the new information is the same as the present, or in the Superdot or Superdash routine in case a 0 is to replace a 1, or vice versa.

We will now describe the operation of the Discriminator, referring to DWG No. 1241.

The lower row of tubes in the drawing consists of one toggle ("$T_1$") and associated gates, used to present information to the toggle and to extract information from it. This toggle is the first element of the circuit affected in each cycle of the Memory: at the time of each Clock pulse, it is cleared to 0, i.e., to the state in which the left half of the 6J6 is conducting. This is accomplished by a clear driver and clear driver-driver circuit, just as in the case of the register toggles.

The next operation in the memory cycle is to turn on the electron beam of the cathode ray tube to inspect the contents of the particular location in the memory tube which is currently of interest. In the "read

regenerate" case this is obviously necessary. In the "write" case it turns out that as we have pointed out before, it is desirable to use different beam turn on routines according as the restoration or changing of the stored information is called for.

Once the Discriminator toggle ($T_1$) has been set, the circuit uses the Discriminator pulse routine pulses to effect when necessary the comparison of the contents of $T_1$ and of the corresponding toggle in $R_1$, and thus to establish the appropriate beam turn on routine. It will be noticed that but a single lead is brought to the Discriminator from the $R_1$ toggle, so that the gating arrangement is somewhat different from that used to read out of $T_1$. Furthermore, this lead does not come directly from the $R_1$ toggle, but from the plate of the Resident digit gate in the Adder; See Fig. 21.

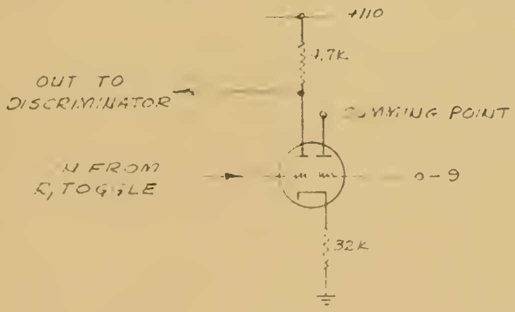


Fig. 21.

Thus, for a $R_1$ toggle grid voltage of -40v (representing a 1), the left section of the Resident digit gate will remain cut off, and the plate voltage will be +110v, this voltage being determined by the bus. A grid voltage of 0, representing a 0, will cause the left section to conduct, and the plate current of approximately 5.5 ma brings the output voltage ($T_2$) to about +84v;

actually this voltage can vary as much as 5 volts either way owing to the resistor tolerance of 10% without causing any difficulty.

The connection to the CRT control grid is made as shown in the upper right-hand corner of DWG No. 1241. The cathode of the CRT is maintained at +318v, so that if the cathode of the 6AL5 is held at or above +288v, the CRT grid is held at +288v, and the electron beam is on. Dropping the grid to +280v is sufficient to cut the beam off, and clearly this can be done by dropping the 6AL5 cathode voltage to slightly below this level. The voltage of the 6AL5 cathode is determined by the 5687 shown in the upper left-hand corner of the schematic. If the right-hand section of this tube draws no current, the grid of the left section will be at +300v and the cathode slightly above this value: this is obviously sufficient to hold the 6AL5 in a non-conducting state and thus permit the CRT electron beam to stay "on". On the other hand, if the right-hand section of the 5687 carries a current of 6 ma, the grid of the left section will drop to +255v: the cathode will be slightly above this, and, therefore, the CRT control grid will fall safely below the cut-off level. Actually about 3 ma would suffice if all the values of resistors in the circuit were precisely as given in the schematic, and not subject to tolerances.

It is, therefore, necessary in all cases to assure that no current is drawn by any of the gates which read out from $T_1$ or from $T_2$ at the beginning of the Inspect pulse.

We shall now establish the waveforms of the pulse trains $SO_1$, $SA_1$, $SO_2$, $SA_2$ which are needed.

First consider the "read-regenerate" case. Here $SO_1$, ..., $SA_2$ must be such that the beam turn on corresponds to the "normal" cases, TT and HH.

There is no reason to consult $T_2$, so both gates to which it is connected must be held in the disabled condition throughout the cycle, which is done by holding $SO_2$ at +70v and $SA_2$ at +120v. This is sufficient to assure us that the left-hand sections of both the $T_2$ output gates will remain in a non-conducting condition.

As far as $T_1$ is concerned, it is definitely known that it initially contains a 0; hence the left-hand gate, which reads out from the right-hand grid of the toggle will not conduct if its cathode is held sufficiently above -35v to assure cut-off, while the right-hand gate will be non-conducting if its cathode is held sufficiently above 0v to assure cut-off. Voltage levels of -10v and +10v are convenient and sufficient for this purpose.

Thus if $SA_1$ = -10v, $SO_1$ = +10v, $SA_2$ = +120v, $SO_2$ = +75v during the Inspect pulse, we will be assured that the CRT electron beam is turned on at the beginning of the pulse time.

During the Inspect time the information stored in the location on the CRT phosphor to which the beam is directed is made available to the Discriminator as follows: the input to grid 7 of the 12AU7 is held at 0v except during the Inspect time when it drops for .5 μs to -25v (the pulse that accomplishes this is called the Strobe). Note that the grids of the 6J6 are biased to -20v and -10v, respectively, so that before the Strobe pulse both sections of the 6J6 are cut off.

During the Strobe we have two possibilities. In case a 0 is read, the signal from the amplifier rises to +5v during the Inspect period; hence, the right-hand grid of the 6J6 rises to -5v, and hence the cathode following it, the left section remains cut-off, and no signal is transmitted to $T_1$. $T_1$ having been just previously cleared to 0, continues to hold a 0. In case a 1

is read, the amplifier output drops from 0v to -20v during the Inspect pulse, thus driving the voltage of the right-hand grid of the 6J6 down to -30v. The cathode voltage drops also, but will be "caught" in the vicinity of -20v as the left section begins to conduct. The plate current of this section, flowing through the 15K plate resistor of the right-hand section of the toggle tube flips the toggle to the 1 condition. Thus by the end of the Strobe pulse, the information held in $T_1$ is identical with that stored in the CRT location that is being read.

Now to continue with the read-regenerate case, there are just two possibilities: either a 0 or a 1 is stored in the given memory location. If it is a 0, the toggle $T_1$ is not flipped during the Strobe time, and hence the CRT electron beam will stay on as long as the values of $SA_1$, ..., $SO_2$ are maintained. These must, therefore, be maintained a length of time correspondint to the Normal Dot. It is convenient to take the quiescent values as follows: $SA_1$ = -10v, $SO_1$ = -10v, $SA_2$ = +120v, $SO_2$ = +70v. Then for Normal Dot (TT) $SO_1$ rises to +10v at the beginning of the Inspect pulse, and returns to -10v at the end of Normal Dot time, which occurs slightly before the end of the Strobe pulse. The other possibility is that the memory location in question holds a 1. Suppose the voltages $SA_1$, ..., $SO_2$ are as determined above. Shortly after beam turn-on, the toggle $T_1$ is flipped. The grid voltage of the left-hand section of the toggle tube now becomes -35v, while that of the right section becomes 0v. As $SA_1$ is -10v and $SO_1$ is +10v, right gate is unaffected while the right-hand section of the left gate now draws plate current of approximately $300/44 \approx 6.82$ ma, which is more than enough to turn off the CRT electron beam. Actually, we would prefer not to turn on the beam at all in the A position, but clearly this must be done in order to ascertain the state

(0 or 1) of the point: it turns out that in the present case the beam is turned off sufficiently rapidly so that not much charge is built up in the A position. Hence, the pulse distribution voltages $SA_1$, etc. that suffice for dot regeneration also suffice for the regeneration of the A position of a dash.

Clearly the B position of the dash must also be regenerated after the twitch. This is done by holding $SO_1$ at -10v, but raising $SA_1$ to +10v for a time equal to the Normal Dash regeneration time: these voltages are clearly adequate to disable the $T_1$ read out gates. We note that in case $T_1$ holds a 0, these values of $SO_1$ and $SA_1$ still permit the left section of the right $T_1$ read out gate to draw 6.82 ma of current, so that in the dot case the beam will stay off after it has been twitched to the B position.

Hence we have shown that for reading and regenerating both 0's and 1's the following modes of variation of the Discriminator pulse routine voltages suffice:

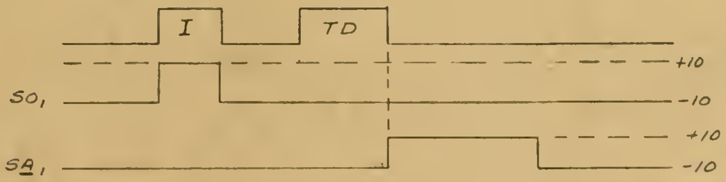


Fig. 22.

During this cycle $SO_2$ and $SA_2$ are maintained at +75v and +120v, respectively.

We now turn to the write case. Here instead of two possibilities we have four, which have already been designated as: TT, HT, HH, TH. Fortunately, a single set of Discriminator pulse routine voltages suffices: we proceed to

derive these.

As before, the CRT electron beam must be turned on in synchronism with the Inspect pulse. The TT case requires, therefore, that $SO_1$ be raised to +10v, and maintained at that level during the time required for dot restoration (Normal Dot). During this time, the level of $SA_1$ is clearly of no consequence, as either of the possible levels will keep the left section of the gate in a non-conducting state. The same is true of $SA_2$. $SO_2$ must be held at +75v during the Normal Dot time.

Now consider the TH case. As in the TT case, the left grid of the toggle tube is at 0v and the right at -35v, while the voltage of the $T_2$ lead is +110v. The CRT beam must be turned on at the beginning of the Inspect pulse, turned off at the expiration of the time required to write the A part of the dash, turned on again at the end of the twitch settling delay, and turned off again at the expiration of the TH pulse (Superdash). $SA_2$ must, therefore, be raised to +120v at the beginning of the Inspect pulse, and dropped back to +100v at the end of the time required to write the A part of the dash. At the expiration of the twitch settling delay, $SO_1$ must be raised to +10v, and $SA_2$ to +120v to assure beam turn on. One, at least, of these voltages must be dropped again at the expiration of the time required for Superdash. We do this to $SO_1$; $SA_2$ can be dropped any time before the beginning of the next cycle. The values of $SA_1$ and $SO_2$ in this case clearly are of no importance: all we have so far determined (from the TT case) is that $SO_2$ must be held at +75v during Normal Dot; it certainly must be raised to +100v at the end of TD, and held there at least until the fall of $SO_1$ for otherwise no current would be drawn from the summing bus during that interval and Normal Dot restoration could not be accomplished.

Thus, so far we have determined the following waveforms for the Discriminator pulse routine voltages:

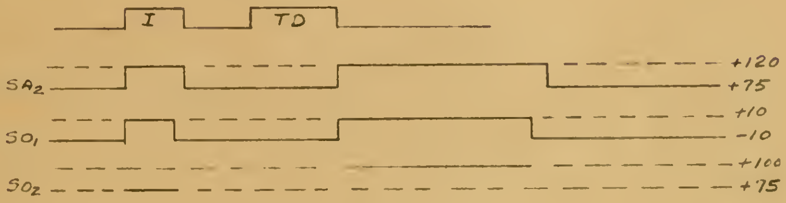


Fig. 23.

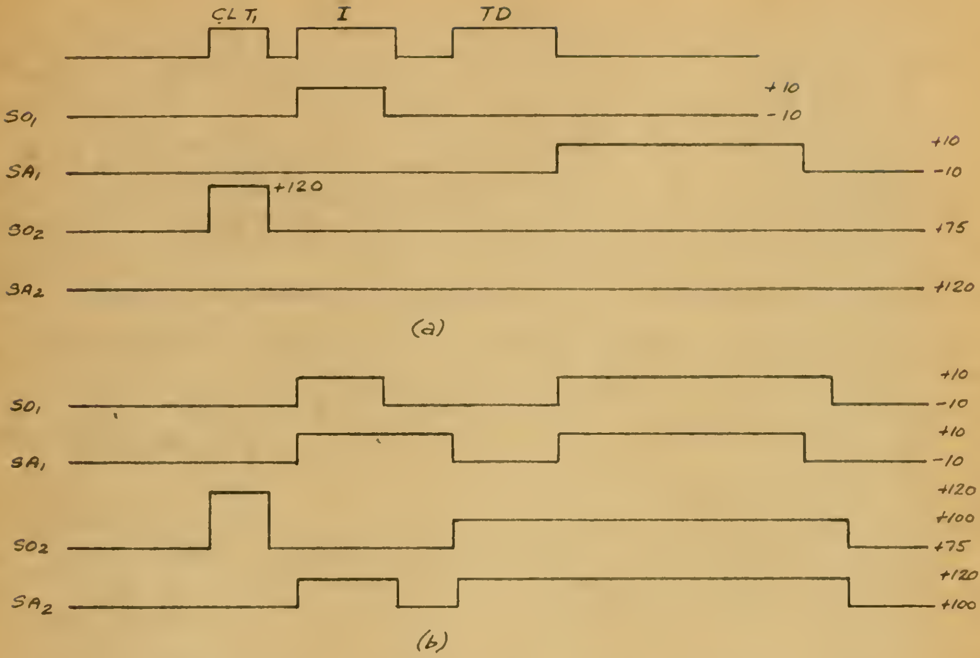
We now turn to cases HT and HH; in both of these the toggle $T_1$ is flipped to the 1 position during the Strobe pulse.

In case HT, the CRT beam must be kept on for Superdot time, which is longer than that required for Normal Dot restoration. This can be done by raising $SA_1$ from -10v to +10v for this period, at the same time holding $SO_2$ at +75v. At the end of this time, either $SA_1$ must be dropped to -10v, or $SO_2$ raised to +100v (we actually do both): Clearly these modes of variation cause no difficulty in the TT and HH routines.

Finally consider case HH. $SO_1$ and $SO_2$ are here important, while the variation of $SA_2$ and $SA_1$ suffice for the restoration of the A position. We also raise $SA_1$ to +10v at the expiration of the twitch settling delay for the time required for normal restoration of the B position. As noted before (under TH) $SO_2$ is raised to +100v during the Superdash interval, so that the beam is guaranteed to be turned on during the shorter Normal Dash restoration period.

Thus we have established the waveforms of the Discriminator pulse routine voltages: Fig. 24 gives the set for (a) the read-regenerate case,

and (b) the write case.

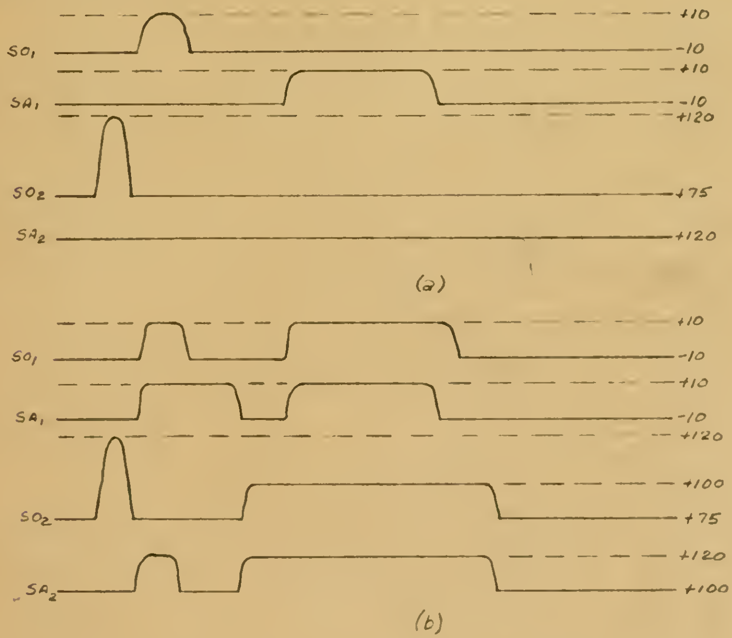


(The time scale in Fig. 24 is such that the duration of "Clear $T_1$" is very nearly 1 μsec.)

Fig. 24.

One slight change must be made to the pattern we have determined, for engineering convenience rather than logical necessity. During the clearing of $T_1$ it is possible that very briefly the grid voltages of the toggle tube are such that no current is drawn from the summing bus by either of the gates. To guarantee that this will not cause beam turn-on, $SO_2$ is caused to rise to +120v during the clearing operation, thus assuring the drawing of current from the summing bus by the $SO_2$ gate. This is shown on our final drawing of the pulse routine voltage waveforms.

Another slight change is made in $SO_2$. It is clearly unimportant whether this voltage remains at +100v or drops to +75v after the completion of the writing of the B part of a dash; it is also unimportant which of these levels it assumes in the brief interval between the Clock pulse and the Strobe pulse, for in both these intervals $SO_1$ and $SA_1$ are -10v, so that we are certain that current is drawn from the summing bus by one of the gates leading out of $T_1$, and that the CRT electron beam, therefore, is cut off. As a matter of convenience $SO_2$ is dropped to +75v at the beginning of the C1 pulse, and kept there until the next Clock pulse, at which time it rises to +120v. It then drops to +75v at the expiration of the Clock pulse; this is shown in Fig. 24.



(The width of the first $SO_1$ pulse is approximately one microsecond).

Fig. 25.

The circuits used to develop the pulse routine voltages which we have been discussing are described in the next section on the Pulse Routine Generator. In Fig. 25 are shown the actual waveforms obtained.

## PULSE ROUTINE GENERATOR

We will now show how the outputs of the pulsers are combined to produce the pulse routine voltages which were shown to be needed for the operation of the Discriminator. The circuits are quite straight forward; a schematic is given in DWG No. 1325.

The inputs to the generator are: TT, TH, HT, HH, Clear $T_1$, I, Cl, TD, and two voltages one of which is -20v for read-regenerate and +10v for write, the other +10v for read-regenerate, -20v for write. The outputs are: $SA_1$, $SO_1$, $SA_2$, and $SO_2$ to the Discriminator, and the twitch pulse, which rises from -20v to +10v with the leading edge of TD, and falls back to -20v with the leading edge of Cl, to the Deflection Generator. The twitch pulse is generated by the toggle labelled "twitch" in the schematic. An output is taken via a cathode follower to the $SA_2$ generator, while the use of the inputs Cl and TD in triggering the toggle are clear from the schematic.

We will now consider the generators of $SO_1$, $SA_1$, $SA_2$, $SO_2$ in order as they appear in the drawing. Reference is made to Fig. 24 where the desired waveforms are shown.

In the write case, the left cathode of the 6AL5 being constantly at +10v and the right one varying with TH, the left grid of the 6J6 is held at -10v except during the TH pulse, when it is raised to +10v. The input to the right grid of the 6J6 is TT, which stays at -10v except during the TT pulse time. The 5687 is, of course, merely a cathode follower. Hence the $SO_1$ output is -10v except during the TT and TH pulses, when it rises to +10v.

During the read-regenerate case, the diode plate is constantly held at -20v, as TH never falls below this level, and hence the cathode of the 6J6 follows the higher grid, which is at all times the right one. Thus, the output is -10v except during the TT pulse, when it rises to +10v.

The operation of the $SA_1$ generator is the same. In the write case the voltage of the left grid of the 6J6 is -10v except during HT, when it rises to +10v, and that of the right grid is -10v except during HH, when it rises to +10v. Hence the output is -10v except during the HT and HH pulses when it is +10v. During a read-regenerate cycle the left grid of the 6J6 is constantly held at -20v, so the output follows the variation of HH, being -10v except during HH, when it rises to +10v.

In the $SA_2$ generator we note that the cathodes of the two 6J6's to which the inputs are applied are connected together, and that the right grid of the right tube is grounded. Thus this section will be cut off if the cathode voltage is above about +5v, under which circumstance the grid voltage of the 5687 is "bumped" at +120v by the right section of the 6AL5; on the other hand, if the right section of the right 6J6 conducts, the input to the 5687 is bumped at +100v by the left section of the 6AL5. In the write case, the right section of the right 6J6 will, therefore, conduct except during I and the time from the beginning of TD to the beginning of C1 when the twitch voltage rises to +10v. Hence the $SA_2$ output in the write case is +100v except during I and the time the twitch voltage is +10v, when it rises to +120v. In the read-regenerate case the right section of the right triode is constantly non-conducting, so the output is constantly +120v.

Finally, we have the $SO_2$ generator; we note that the inputs are applied to a 6J6 at the left and to one at the right, which appears just above the

5687 cathode follower in the schematic. This second 6J6 is so arranged that its left section conducts except while the Discriminator toggle $T_1$ is being cleared: thus, the voltage of the right grid of the center 6J6 is held at somewhat below +60v except during Clear $T_1$ when it rises to +120v. We observe that the voltage of the left grid of the 6J6 in the center is constrained by the 6AL5 bumper to lie between +75v and +100v. Hence in all cases the output voltage $SO_2$ must rise to +120v during the Clear $T_1$ (or Clock) pulse, and at no other time can it exceed +100v. Now consider the left 6J6. During a write cycle its left section is obviously held in a cut-off condition, while its right grid is held at -20v from the beginning of TD to the beginning of Cl, when it rises to +10v, where it remains until the beginning of the next TD pulse. Thus from the beginning of TD to that of Cl, the voltage of the left grid of the center is +100v, while the rest of the time it is +75v. Thus $SO_2$ is +120 during Cl $T_1$, at the end of which it falls to +75v where it remains until TD, when it rises to +100, falling again to +75v at the beginning of Cl.

Comparison with the waveforms deduced as necessary for the operation of the Discriminator (Fig. 24) shows that the circuits we have been discussing should produce these subject to finite times of rise and fall of the pulses. The actual waveforms obtained are shown in Fig. 25. The rise times of the pulses are approximately .25 $\mu$s in all cases; no serious distortion is present, but a delay of approximately .05 $\mu$sec is introduced by the circuits which is obviously too small to show in the drawings.

## WILLIAMS TUBE DEFLECTION GENERATOR

We have seen that each storage tube holds an array of 32 x 32 bits of

information. The address of a bit consists of two numbers, each being one of the integers 0, 1, ..., 31 (each, of course, expressed in binary notation) which specify the horizontal and vertical coordinates of the bit.

An address is presented to the memory organ as the contents of a ten stage binary register, the stages $2^0$, $2^1$, ..., $2^4$ specify the horizontal coordinate, and $2^5$, ..., $2^9$ the vertical one. These binary numbers must be converted into the voltages needed to deflect the electron beam: this is the function of the Deflection Generator, a schematic of which appears in DWG. No. 1284 and DWG No. 1285. Before going on to a description of the operation of this circuit, it should be mentioned that the twitch is treated as an extra digit column in the horizontal coordinate: $2^0$ is treated as the highest order column, $2^1$ the next and so on, with the twitch of order lower than $2^4$.

The terminals at the bottom of DWG No. 1284 present to the deflection generator the twitch voltage (a pulse rising from -20v to +10v in synchronism with the rise of TD, and falling again in synchronism with the leading edge of C1), and the digits of the address (+5v for a 0, -30v for a 1). The latter values are due to the fact that connections to the input terminals come from the address register by coaxial cable, which is driven by a cathode follower the input of which is taken from a toggle grid; cathode rise of 5v in the cathode follower accounts for the values quoted here.

In order to minimize noise that may enter the deflection generator, the full variation available at each input terminal is not used, the diode bumper, which is shown as the tube at the bottom of the left column in DWG No. 1284 restricting the swing to ~~one~~ from 0v to -10v (these are, therefore, the nominal values for 0 and 1, and for twitch on and twitch off).

Now consider the 6J6 that appears just above the input bumping diode. As its left grid is held at -5v, the left section will be non-conducting when the right grid is raised to 0v, but conducting when the right grid is dropped to -10v. In the former case, the voltage at the right grid of the second 6J6 (fourth tube up) is bumped at +120v by the 6AL5. In the latter, it is bumped at +100v (we note that the plate current of the left section of the first 6J6 must be somewhat greater than 95/13000 ≑ 7.3 ma, so that the plate voltage will surely fall below +100v).

The second 6J6 in the column has, therefore, as input to its right grid +120v for twitch on, +100v for twitch off. As its left grid is held fixed at +110v, the left section will not conduct in the first case, but will in the second, drawing a plate current of somewhat over 4.07 ma. As regards the right section, the situation is reversed: in the first case a plate current of somewhat over 4.44 ma is drawn, in the second it is cut off.

Hence the voltages of the left and right plates of the 6J6 are, respectively, for twitch on, 400v, 382.7v; for twitch off, 384.1v, 400v.

In the first case the 12AX7 in the upper left-hand corner of the drawing will have its left section on and its right section off; in the second case the reverse will be true. Thus it will draw a current I = 100/R (where R is the resistance in the cathode circuit) from summing bus A, and none from B, while in the second these will be interchanged. In practice the variable 500K resistor is adjusted to maximize the amplitude of the dash output of the Williams Memory Output Amplifier, which depends upon the magnitude of the displacement between the A and B positions.

The operation of the other columns of tubes, which exactly duplicate the one we have discussed in detail, except for the tube type and the value of

the cathode resistor of the top tube in the column, is, of course, identical with that of the first column except as regards the current drawn from the summing buses A and B. Thus in each case a 0 input to the column results in the drawing of approximately 100/R amperes from bus A and no current from B, while for a 1 input these will be interchanged. Taking account of cathode rise in each of the tubes, the design values of the cathode resistors were chosen so that the $2^0$ stage would draw $i_0 = 6.98$ ma; stage $2^1$, $i_1 = 1/2\ i_0$ ...; stage $2^4$, $i_4 = 1/2^4\ i_0$. These currents are added in the summing buses, the object being, of course, ultimately to cause them to flow through a resistor, so that the voltage developed across this will be proportional to the binary number used as input to the generator.

However, it is desired to make the currents developed available at a higher voltage level (+1290v). This cannot be done merely by connecting resistors in series with the summing buses directly to the +1290v voltage as this would cause the tubes whose plates are connected to the buses to operate with excessive plate voltage, so a rather simple scheme, consisting of four triodes in series for each bus, was adopted. This is shown in DWG No. 1285. Here we have two columns of 5687's, giving, therefore, four columns of triodes; the cathodes of the tubes of the row at the bottom of the drawing are connected to the four summing buses A, B, C, D of DWG No. 1284. The grid voltages are held at +496v, +684v, +872v, and +1060v by means of the voltage divider, consisting of a 40K, three 33K, two 27K, and a 33K resistor connected between +1290v and ground. Condensers are placed in parallel with the resistors so that when the high voltage is turned on the grids will instantaneously assume their correct potentials. The parallel RC circuits between the points feeding the grids and the heaters, hold the heaters at the d.c.

level of the grids, so that the potential difference between each cathode and its heater will be small. The condensers guarantee that the heaters assume the desired potentials instantaneously when the high voltage is turned on.

The top triode in each column is connected through a 3.8K resistor to the +1290v bus. Each summing bus current flows through one of these, and hence there is developed across it a voltage proportional to this current. The voltages at the lower end of these resistors are the deflection voltages: thus A and B drive the horizontal deflection plates of the CRT's, and C and D the vertical plates. Each deflection voltage is applied to all forty CRT's in parallel by means of a deflection bus. The two cathode followers in cascade shown in the upper left-hand corner of DWG No. 1285 provide the low impedance source needed to drive the rather large capacity of this bus.

We observe that a 0 in any digit position of the horizontal address causes the drawing of current from the A bus, while a 1 causes it to be drawn from the B bus. For the vertical deflection system, a corresponding remark is true of C and D. Suppose the horizontal address is 00000. Then i(1 + 1/2 + 1/4 + 1/8 + 1/16) ≑ 13.52 ma is drawn from the A bus, and 0 ma from the B bus, and the deflection plate voltages are +1238.6v and 1290v, respectively: These are, of course, reversed in the case of the address 11111; in both cases the average value is +1264.3v, or 25.7v below +1290. This condition holds for all addresses, as the average of the two deflection voltages must always be 1/2 (1290 + 1290 - i(1 + 1/2 + 1/4 + 1/8 + 1/16) x 3.8), where i is in milliamperes; the design criterion here was to hold the point half way between the deflection plates constantly at the same potential as the second anode. Clearly, it is necessary that we consider both the horizontal and the vertical deflection plates: the potential of the point must be the same when referred

to either set of plates. The circuits shown in DWG No. 1284, labelled "Average Deflection Plate Level Adjustment" permit these potentials to be equalized. Moreover, these circuits guarantee that some current is flowing in the buses A, B, C, D, at all times, so that the tubes in the vertical chain are never operated very close to cut-off, and hence always in the region where the characteristics are linear.

## WILLIAMS MEMORY LOCAL CONTROL

A single chassis contains both the Pulse Routine Generator, which has already been described, and the Williams Memory Local Control. It also includes circuits, shown in DWG No. 1325 and 1339, for generating -B, -TD, and the Strobe (which is an inverted and magnified version of the Inspect pulse (I)). The Local Control schematic is given in DWG No. 1339, to which reference is made. A block diagram is given in Figure 26.

Generally speaking, the Local Control receives from the Main Control signals which signify whether or not the Memory is to be consulted in the next cycle, and whether information is to be inserted in or extracted from it. It uses this information to cause the routine generators to emit the appropriate pulse trains, and to route back to the Main Control properly timed pulses, originating in the Pulsers, which the Main Control can use to clear RIII, open gates into RIII, and to gate address information out of either part of the order counter or from $R_3$ to the Williams Tube deflection circuits as may be desired. Local Control also returns to Main Control signals acknowledging the request to use the Memory, and showing that the process ordered has been completed. The Local Control serves to coordinate the generally asynchronous operation of the rest of the computer with the carefully timed operation of the Williams Memory.

The inputs to the Local Control come from two sources: the Main Control and the Pulsers. Main Control supplies the Yes/No and Read/Write signals, both toggle outputs assuming levels of 0v and -30v. "Yes" signifies that the Memory is to be consulted during the next cycle, which is, therefore, called an "action" cycle, while "No" signifies that the Memory will not be consulted and that a regeneration cycle will, therefore, ensue. Ordinarily, action and regeneration cycles follow each other in sequence, the one exception being in the case of that type of action cycle which we shall call a "fetch" cycle, which occurs whenever the second order in the word standing in $R_3$ has been executed and it becomes necessary to bring the next pair of orders from the Memory to $R_3$. In this case it is permitted that a fetch cycle be followed by a second action cycle. To assure that an action cycle is to follow a regenerate cycle the Yes signal must be received before the $TD_t$ pulse of the regenerate cycle, while the Read/Write information must be received before the time of the B pulse. We shall see that the Yes/No toggle is always set to No by the Acknowledge Yes pulse emitted by the Local Control at the time of this same B pulse. If an action cycle is to follow a fetch, it is necessary that a Yes signal be received before the $\bar{A}$ pulse of the fetch cycle.

The remaining inputs to the Local Control are received from the Pulsers, or are built up locally from them: thus $TD_t$, $\bar{A}$, Cl, $Cl_{T_1}$, are used directly, while other circuits shown in DWG No. 1339 invert B and TD to provide inputs of -B and -TD.

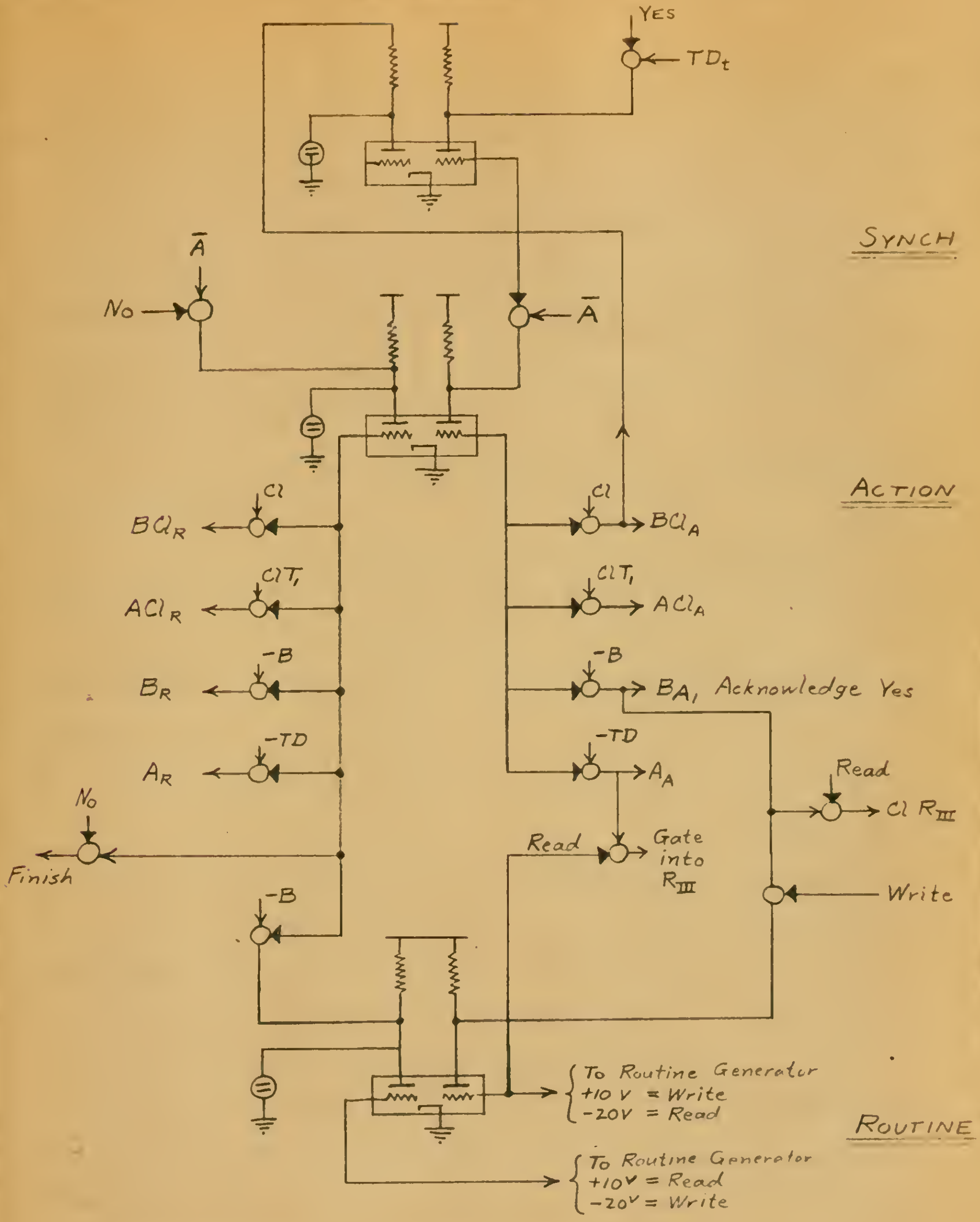
The outputs of the Local Control are: $A_A$, $B_A$, $ACl_A$, $BCl_A$, $A_R$, $B_R$, $ACl_R$, $BCl_R$, "Finish", "Acknowledge Yes", "ClRIII," "Gate into RIII" to the Main Control, and a "Write/Read" signal to the Pulse Routine Generator (the first eight of these are used to operate the Dispatch Counter in the Main Control).

Circuitwise, the Local Control consists of three toggles and a rather complicated system of gates. The operation of the circuit can best be made clear by reference to the logical block diagram given in Fig. 26. We use in it the conventional representations of the toggle as a box and of the gate as a circle with two arrowhead inputs and one output. An input to a gate from a grid of a toggle signifies that the gate is enabled when the grid is high, but disabled when the grid is low. In the actual circuit the arrangement is slightly different, in order to take advantage of different gating arrangements needed to give different voltage outputs, but once the logical structure is understood, the schematic (DWG No. 1339) will be found readily comprehensible. Note that the Action and Routine toggles differ slightly from those used throughout the machine in that the crossover resistors are each replaced by two resistors in series, the output being taken from the point between them. This results in an output of +10v from the conducting half of the toggle tube, and of -20v from the non-conducting half.

Having disposed of these preliminary remarks, we now turn to an explanation of the operation of the Local Control, basing our argument on Fig. 26.

Let us assume that the Synch, Action, and Routine toggles are all in their 0 states; i.e., the neon bulbs are not glowing.

Suppose that an action cycle is called for, signified by the Yes/No input assuming its Yes level before the arrival of $TD_t$. Then the gate into the Synch toggle is enabled, and $TD_t$ causes this toggle to assume its "on" state (neon bulb glowing). This in turn enables the gate into the Action toggle, which is turned on by the $\bar{A}$ pulse. The grid of the right-hand section of the Action toggle tube now is high (+10v) while that of the left-hand section is low (-20v), and the gates connected to the right-hand grid are enabled, while



Wm. LOCAL CONTROL LOGICAL BLOCK DIAGRAM

FIGURE 26

those connected to the left-hand grid are disabled. Thus the following sequence of events ensues:

1) $BCl_A$ is emitted, and the Synch toggle turned off;

2) $B_A$ and Acknowledge Yes are emitted, the latter returning the Yes/No toggle in the Main Control to the No condition; furthermore, if Reading is called for, $B_A$ is passed on as ClRIII, and the Routine toggle left in the Read condition, while if Writing is called for, $B_A$ flips the Routine toggle to the Write condition:

3) $ACl_A$ is emitted in synchronism with $Cl_{T_1}$, at the beginning of the next memory cycle;

4) $A_A$ is emitted in synchronism with TD of the next memory cycle; if Reading is called for, $A_A$ also causes "gate into RIII" to be emitted;

5) The Yes/No toggle having been set to No, the left gate into the Action toggle is open, and the toggle is turned off by $\bar{A}$, thus enabling the whole set of gates in the left column;

6) The Finish signal is emitted;

7) $BCl_R$ is emitted;

8) $B_R$ is emitted, and the Routine toggle set to the off (Read) condition if it is not already in that condition; thus the performance of an ensuing Regenerate cycle is assured;

9) $ACl_R$ is emitted in synchronism with $Cl_{T_1}$;

10) $A_R$ is emitted in synchronism with TD.

Thus we see that ordinarily a Regenerate cycle follows an Action cycle; however, in the case of a fetch, the Yes/No toggle is set to Yes before $\bar{A}$ in the fetch cycle, which prevents the turning off of the Action toggle, and thus assures that the subsequent cycle will also be one of action. We note that in

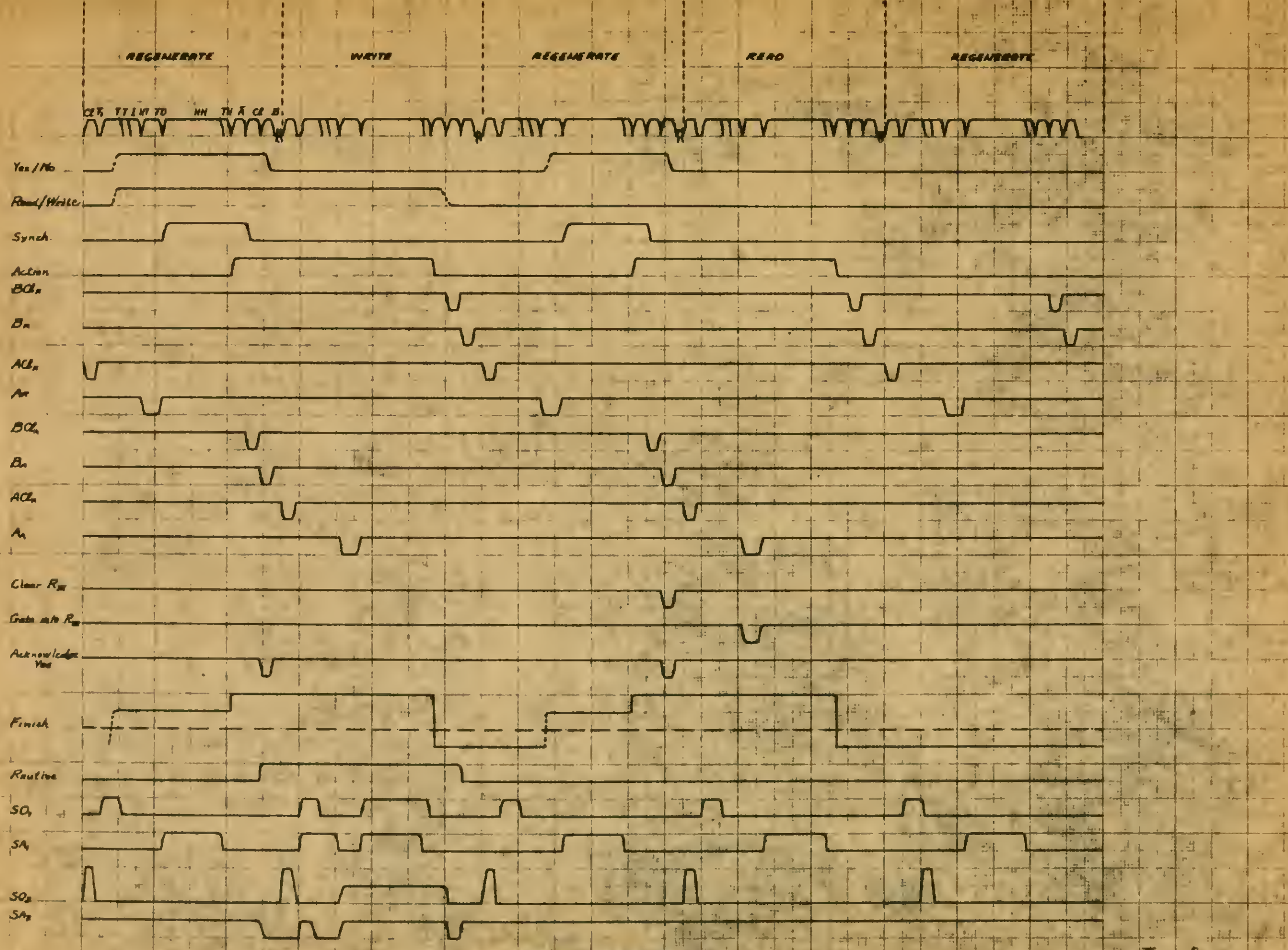
our sequence of events, after 8) all the toggles have been set to their off condition and will remain so at least until after 10), since if an Action cycle is to be called for, the Synch toggle cannot be turned on until $TD_t$.

Complete diagrams are given in Figures 27 and 28 illustrating the operations that have just been described. Fig. 27 shows the time variation of the voltage inputs and outputs for the following sequence of cycles: Regenerate, Write, Regenerate, Read, Regenerate. Fig. 28 does the same for the sequence: Regenerate, Fetch, Write, Regenerate.

## IV. THE MAIN CONTROL

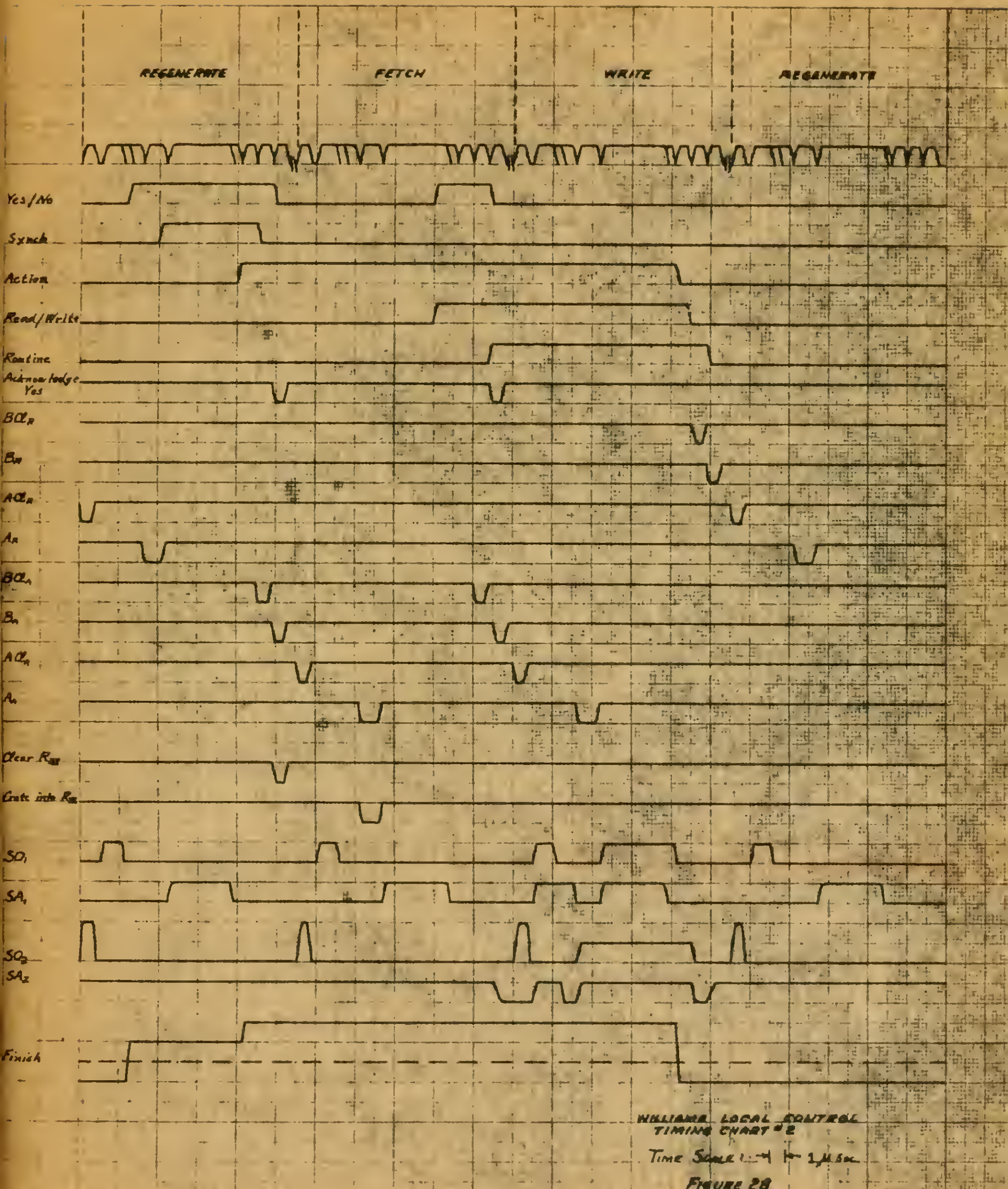
We have described the Williams Memory in some detail, and have shown how the Local Control regulates its operation subject to information received from the Main Control. This information must be of two kinds. First, it is necessary to specify whether an Action or a Regenerate cycle is to be performed, and whether information is to be inserted in or extracted from the Memory. Second, it is necessary to supply to the deflection circuits the address in the Memory of the bits of information which are to be written, read or regenerated. The equipment needed to decode that part of each order which specifies the Yes/No and Read/Write alternatives was not yet completed while this report was being written. The Dispatch Counter, which supplies address information to the deflection circuits, was completed and installed, and will be described below.

Besides supplying orders and address information to the Memory Organ, the Main Control also must regulate the actions of the Input-Output Organ and of the Arithmetic Organ. Most of the equipment for the latter function has been built and installed, and will be described under the headings "Gate-Clear Sequencing Chain", "Shift Counter", and "Recognition Circuits". Obviously



WILLIAMS LOCAL CONTROL TIMING CHART #1

FIGURE 27



WILLIAMS LOCAL CONTROL
TIMING CHART #2

Time Scale ⊣ ⊢ 1 μSec

Figure 28

our account of these circuits will be rather fragmentary, and it will be necessary to show in a later report, once the remaining portions of the Control have been completed, how the separate parts are connected into an integrated unit.

## THE SHIFT COUNTER

Two types of counter are used in the present machine. These are the familiar "scaling" type, of which the Shift Counter is an example, and the "adder" type, which operates as an Adder to which one input is the last count and the other is a 1 to the lowest order stage. The Scaling type of counter has the advantage that the more significant stages can be comparatively slow, and that all the carries resulting from one count need not be completed before the next count arrives at the input, whereas in the Adder type, all carries resulting from one count must be completed before the next count is added. On the other hand, the Adder type offers the advantage of requiring fewer tubes. Hence, the character of the particular application indicates the appropriate type of counter. In the Dispatch Counter the complete new address must be obtained before the counter is stepped again, so that the Adder type is obviously appropriate, while in the Shift Counter this is not true, so that the Scaling type is used.

The Shift Counter is part of the equipment used to control the carrying out of the arithmetical processes. Thus multiplication is performed by successive additions and shifts. Once the process is initiated, the Shift Counter counts the successive shifts. The number of these which must be performed is inserted in the Recognition circuit, where it is continuously compared with the contents of the Shift Counter; when coincidence is indicated,

a signal is emitted which terminates the process. A similar situation occurs in the carrying out of division.

Physically the Shift Counter consists of two rows of toggles with gates permitting information to be transferred up and down vertically and up diagonally. One row of toggles holds the actual count, the other does not; these are referred to as the True and False rows, and the numbers they hold as the True and False counts, respectively. It will appear that the False count does not proceed monotonically. There are six stages in the counter, those for $2^0$, $2^1$, ..., $2^5$. Since the counter must only count to forty (the number of additions inthe multiplication process) the $2^5$ stage can be rather simpler in structure than the lower order stages; it is feasible to have but a single toggle in this sixth stage.

Before examining the schematic of the counter, let us consider the block diagram of a single stage, given in Fig. 29(a). This represents any of the stages $2^0$ to $2^4$. It has already been remarked that the sixth ($2^5$) stage is of simpler structure; it will be considered later. Here input $E_n'$ enables gates from the True to the False toggle, which are so arranged that the enabling of the gates causes F to assume the same condition as T. On the other hand, input $E_n''$ enables gates leading from F to T in such a way that the enabling of the gates causes T to assume the condition opposite to that of F. At the input to the $2^0$ stage, the levels for $E_o'$ are 0v to disable, -20v to enable, while those for $E_o''$ are +60v to disable, +110v to enable; in the following stages the levels of $E_n'$ become 0v and -35v, and those of $E_n''$ remain substantially unchanged. We will have more to say on this subject when we discuss the circuitry.

The input to the lowest order ($2^0$) stage of the counter consists of

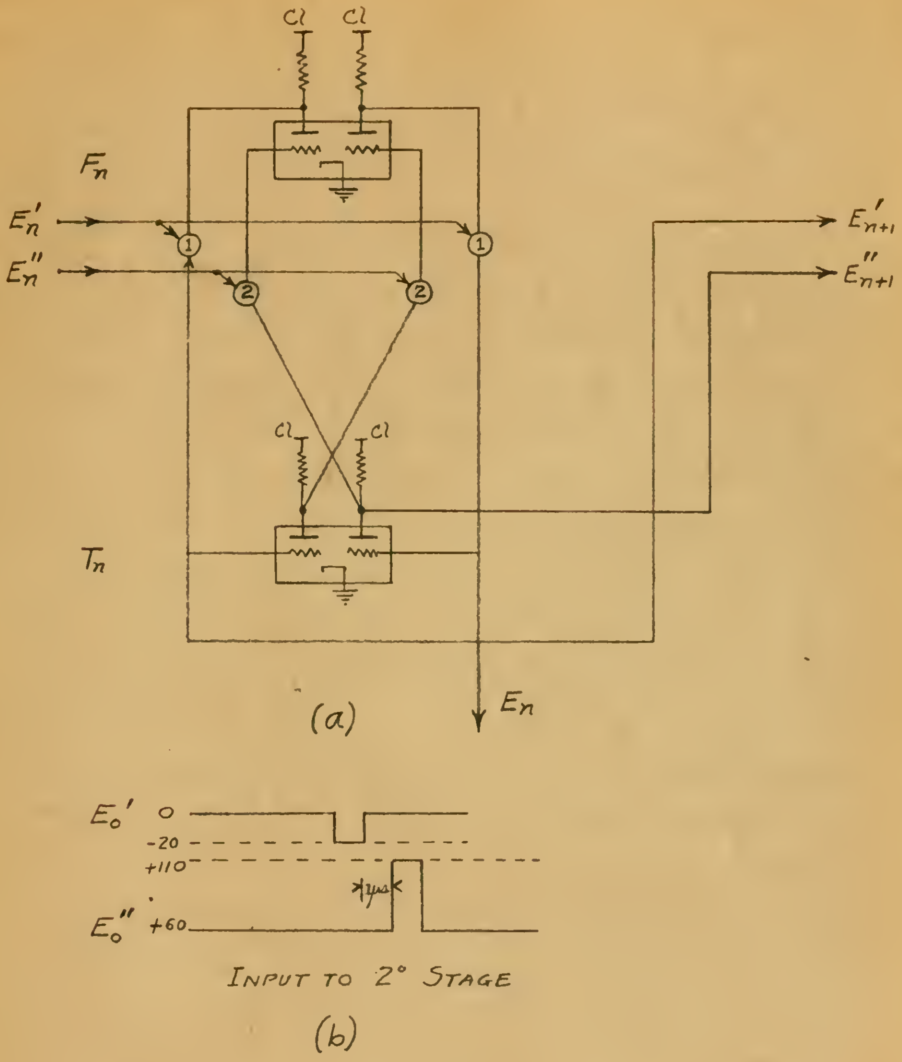

Cl
Cl
$F_n$
$E_n'$
$E_n''$
1
1
2
2
$E_{n+1}'$
$E_{n+1}''$
Cl
Cl
$T_n$
$E_n$
(a)
$E_0'$
0
-20
+110
1μs
$E_0''$
+60
INPUT TO 2° STAGE
(b)

FIGURE 29

the pair of pulses shown in Fig. 29(b) for each item to be counted. The number held by the counter is presented to the recognition circuit, which is physically located on the same chassis, as a set of six voltages, one for each stage of the counter, the presence of a 0 being signified by 0v, that of a one by -40v.

Each stage of the counter, therefore, has two inputs and three outputs; on Fig. 29(a) the inputs are designated $E_n'$ and $E_n''$, the outputs $E_n$, $E'_{n+1}$, $E''_{n+1}$. Of these $E_n$ signifies to the recognition circuit the contents of the stage, while $E'_{n+1}$, $E''_{n+1}$ are inputs to the next stage. In the actual circuit, DWG No. 1289, let us label the tubes Tij, where i signifies the row and j the column in the array. The first five columns and the lower three tubes of the sixth form the actual counter. The upper four tubes in the sixth column are clear drivers used to clear the two rows of toggles. Consider the first column. $T_{11}$ is the F toggle of the block diagram, $T_{21}$ is the up gate, $T_{41}$ the down gate, $T_{31}$ the gate driver, while the lower three tubes, $T_{51}$, $T_{61}$, $T_{71}$ are the T toggle, which is actually what we have before termed a Supertoggle. It is used in this instance because of the speed with which it can be caused to switch from one state to the other.

The counter is prepared for operation by clearing all the T toggles to 0 and the F toggles to 01111 ($2^0$ holding a 0, the others 1's). Consider the first column. The first pulse of the input pair clearly does nothing, for in this case both T and F already hold 0's. On the other hand, the down gates transmit a 1 to T if F holds a 0. Hence after the reception of the pair of pulses T holds a 1.

Now let us consider the influence of the n-th column of the counter

upon the (n+1)-th. According to the block diagram of one stage, the gating voltages (1) and (2) to the next stage are the left grid and right plate voltages of the $T_n$ toggle tube. Hence while this toggle holds a 0, (1) and (2) are both at their high level with the result that in the next column the up gates are disabled and the down gates enabled. On the other hand, when $T_n$ holds a 1, the gating voltages are both held at their lower values, with the result that the up and down gates of the next stage are, respectively, enabled and disabled.

Thus if $T_n$ holds a 0, $T_{n+1}$ must hold a 1 or a 0 if $F_{n+1}$ holds a 0 or a 1, while if $T_n$ holds a 1, the contents of $F_{n+1}$ must coincide with that of $T_{n+1}$. These facts mean that whenever $T_n$ holds a 0 its next change of condition to 1 cannot change $T_{n+1}$, but does cause $F_{n+1}$ to agree with $T_{n+1}$, while whenever $T_n$ holds a 1, its next change of condition to 0 cannot affect $F_{n+1}$, but must cause a change of condition in $T_{n+1}$. Thus two successive changes of condition in $T_n$ cause a single change of condition in $T_{n+1}$, so that the performance of the circuit as a binary counter of the scaling type is guaranteed.

We will now consider the actual circuits involved, and in particular will show how the simplified sixth stage of the counter works, and how its simplified form restricts the number of items that can be counted without impairing the usefulness of the counter in its particular application.

The toggles of the False rank and that in the sixth stage of the True rank are of the type encountered throughout the computer, while the first five toggles of the true rank are the so-called Supertoggles. The gating arrangement from T to F is quite straightforward; we describe it for the first column, the remarks obviously also applying to all others but the sixth. Each gate consists of one section of $T_{21}$ and the left section of $T_{31}$. From

the way in which the grids of the toggle tube $T_{61}$ are returned to -300v, it is readily seen that when the voltage of a grid of the toggle tube is 0v, that of the corresponding grid of the gate tube $T_{21}$ is approximately -10v, while when the toggle grid voltage is -40v, that of the gate grid is approximately -48v. Hence, if the grid of the left section of $T_{31}$ is held at 0v, it is clear that the cathode of $T_{21}$ is held so far above that of either grid that conduction is impossible, while if the grid voltage of the left section of $T_{31}$ is dropped to either -20v or -40v, that section of $T_{21}$ will conduct, the grid voltage of which is 0v, while the other section will remain cut off.

Now consider the "down" gates, each composed of the right section of $T_{31}$ and one section of $T_{41}$. The grid voltages of $T_{41}$ are either 0v or -40v, while its cathode is returned to ground, and both plates are connected to the right cathode of $T_{31}$ through 5.6K resistors. While the voltage of the right grid of $T_{31}$ is held at 60v, that of the plate of the conducting half of $T_{41}$ is substantially below 60v (apart from cathode rise in $T_{31}$). The plates of $T_{41}$ are connected to the left grid of $T_{51}$ and the right grid of $T_{71}$, the other grids of these tubes being connected to the plates of the Supertoggle tube, $T_{61}$. Hence, while the gating voltage $E_o''$ is held at 60v, neither plate of $T_{41}$ is effective in determining the cathode voltage of $T_{51}$ or $T_{71}$, and the Supertoggle can remain in either condition.

Now suppose the voltage (2) to be raised to +110v, bringing with it the voltage of the plate of the cut-off section of $T_{41}$. Let us assume that $F_1$ holds a 0, so that this is the right section of $T_{41}$: the plate voltage of the left section also rises to about 60v. Suppose now that $T_1$ holds a 1, so that the grid voltage of the right section of $T_{51}$ is about +60v, and that of the left section of $T_{71}$ is +110v. The grid voltages of the left section

of $T_{51}$ is about +60v, and that of the left section of $T_{71}$ is +110v. The grid voltages of the left section of $T_{51}$ and the right section of $T_{71}$ are also +60v and +110v, respectively, so clearly nothing happens. On the other hand, if $T_1$ holds a 0, the grid voltages of the right section of $T_{51}$ and the left section of $T_{71}$ are +110v and +60v, respectively, and, therefore, the cathode voltage of $T_{71}$ is raised to +110v, the voltage of the right grid. Clearly this flips the supertoggle to the 1 position. Similarly, if $F_1$ holds 1 and $T_1$ 0, the raising of the gating voltage $E''_0$ from +60v to +110v does not affect $T_1$, but if $T_1$ holds 1, it causes it to flip to 0.

The discussion just given applies to the columns $2^0$, ..., $2^4$. The $2^5$ column is simpler in structure, consisting of three 2C51 tubes: $T_{56}$, $T_{66}$, $T_{76}$, of which $T_{66}$ is the toggle tube, the other two performing gating functions. Inputs are: from the left grid of $T_{65}$ to the left grid of $T_{76}$, and from the right grid of $T_{65}$ to the left grid of $T_{56}$.

Suppose 0's exist in the $2^4$ and $2^5$ stages. Then the left section of $T_{56}$ is cut off, and the right conducting, the cathode voltage being -40v. The left section of $T_{76}$ is conducting, the cathode being 0v. Now consider the right section of $T_{76}$, which is connected as a diode. The plate is connected through a 4.7K resistor to the cathode of the left section, and the cathode is connected directly to the cathode of the right section of $T_{56}$. Hence, the right section of $T_{76}$ conducts, and its plate voltage, which is the output from this stage to the recognition circuit, is not much above -40v.

Now let the $2^4$ stage toggle flip to 1. The cathode of the left section of $T_{76}$ now falls to -40v, and as the cathode of the right section cannot fall below this voltage, the output remains at -40v. The left section of $T_{56}$ conducts, and the usual gating action takes place, the toggle being flipped to the 1

condition. Thus flipping the toggle in the $2^4$ stage to 1 automatically flips the toggle in the $2^5$ stage, but does not effect the output voltage, which remains -40v, signifying a 1.

This condition persists as long as the $2^4$ stage holds a 1, hence, up to and including the count of 31. On the count of 32, stages $2^0$, ..., $2^4$ must all return to 0. The left section of $T_{56}$ is now cut off leaving the toggle in the 1 condition, and the cathode of the right section, and hence the cathode of the right section of $T_{76}$, rises to 0v. At the same time the cathode of the left section of $T_{76}$ rises to 0v, and we are assured that the right section of $T_{76}$ will not conduct, and its plate voltage, therefore, becomes 0v, signifying a 1 to the recognition circuit.

The lower order stages now proceed with the count, the $2^4$ stage remaining in the 0 condition until the count of 48, when it flips to 1. We have already seen, however, that if both the $2^4$ and $2^5$ stage toggles are in the 1 condition, the $2^5$ stage output voltage drops to -40v, signifying a 0 to the recognition circuit. The shift counter can only count to 47, returning to 32 on the count of 48. However, since the Shift Counter is only required to count to 40, this is no limitation on its usefulness. The recognition of this fact permits the simplification of the $2^5$ column, with attendant saving in tubes. The space thus saved is occupied by the two clear drivers $T_{16}$, $T_{36}$, and the cathode followers $T_{26}$, $T_{46}$: $T_{26}$ permits all the plate current for the F toggles to be drawn from the +240v bus, thus holding this current constant and preventing any fluctuation of plate voltage due to current fluctuation in the power supply and bus impedance, while $T_{46}$ accomplishes the same for the T toggles and the +220v bus.

Fig. 30 shows the contents of the F and T toggles as the counter proceeds from its quiescent condition to the count of forty. In the $T_5$ column

| $n$ | $T_0$ | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_5$ | $F_0$ | $F_1$ | $F_2$ | $F_3$ | $F_4$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 8 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 10 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 13 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 14 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 16 | 0 | 0 | 0 | 0 | 1 | [1] | 1 | 1 | 1 | 1 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 | [1] | 0 | 0 | 1 | 1 | 0 |
| 18 | 0 | 1 | 0 | 0 | 1 | [1] | 1 | 0 | 0 | 1 | 0 |
| 19 | 1 | 1 | 0 | 0 | 1 | [1] | 0 | 1 | 0 | 1 | 0 |
| 20 | 0 | 0 | 1 | 0 | 1 | [1] | 1 | 1 | 0 | 0 | 0 |
| 21 | 1 | 0 | 1 | 0 | 1 | [1] | 0 | 0 | 0 | 0 | 0 |
| 22 | 0 | 1 | 1 | 0 | 1 | [1] | 1 | 0 | 1 | 0 | 0 |
| 23 | 1 | 1 | 1 | 0 | 1 | [1] | 0 | 1 | 1 | 0 | 0 |
| 24 | 0 | 0 | 0 | 1 | 1 | [1] | 1 | 1 | 1 | 0 | 1 |
| 25 | 1 | 0 | 0 | 1 | 1 | [1] | 0 | 0 | 1 | 0 | 1 |
| 26 | 0 | 1 | 0 | 1 | 1 | [1] | 1 | 0 | 0 | 0 | 1 |
| 27 | 1 | 1 | 0 | 1 | 1 | [1] | 0 | 1 | 0 | 0 | 1 |
| 28 | 0 | 0 | 1 | 1 | 1 | [1] | 1 | 1 | 0 | 1 | 1 |
| 29 | 1 | 0 | 1 | 1 | 1 | [1] | 0 | 0 | 0 | 1 | 1 |
| 30 | 0 | 1 | 1 | 1 | 1 | [1] | 1 | 0 | 1 | 1 | 1 |
| 31 | 1 | 1 | 1 | 1 | 1 | [1] | 0 | 1 | 1 | 1 | 1 |
| 32 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 33 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 34 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 35 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 36 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 37 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 38 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 39 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 40 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

FIGURE 30

the symbol $\left[1\right]$ is used to indicate that, though the toggle is in the 1 condition, the output is so arranged as to present a 0 to the recognition circuit.

## RECOGNITION CIRCUIT

The function of the Recognition Circuit is to compare the number in the True rank of toggles in the Shift Counter with some predetermined number, to determine when the two coincide, and at that instant to emit a signal which can be used to terminate the process the number of steps in which is being counted.

Since the "number to be recognized" and the number in the counter are both six place binary numbers, there are twelve inputs to the Recognition Circuit. Six of these are the output leads from the True rank of Counter toggles, and six come ultimately from the read-out gates of $R_3$. There is a single output, the signal emitted when the number in the counter has increased until it coincides with the "number to be recognized."

The Shift Counter chassis contains the Recognition Circuit, and also the Address Dispatch Gates, which will be described later on. We refer to DWG No. 1289 for the schematic.

The Recognition Circuit itself consists of the the last six tubes in each of the two lowest rows in the drawing: $T_{67}, \ldots, T_{6,12}$, and $T_{77}, \ldots, T_{7,12}$. The inputs labelled (A) are clearly from the Shift Counter, while the voltages representing the "number to be recognized" are brought down on the leads labelled (B), these voltages being developed in the cathode circuits of the input cathode followers $T_{2,8}, \ldots, T_{2,12}$.

Each of the tubes $T_{2,8}, \ldots, T_{2,12}$ is a 2C51, the two sections functioning independently as cathode followers. We observe that each grid is

connected to the +110v bus through a 7.5K resistor and to the input lead from $R_3$. The 110v bus is the plate supply of the RIII Green gates. Since all ten cathode follower circuits are identical, let us consider one in detail.

Suppose, for example, that the $2^0$ toggle in $R_3$ contains a 0. Then the opening of the RIII read out (Green) gate has no effect on $T_{2,8}$, since no current is drawn from the +110v bus. The voltage of the left cathode is +110v, and, if the grid of the left section of $T_{3,8}$ were not connected to the point between the 15K and the two 22K resistors in the cathode circuit, the voltage of this point would be approximately +6v. With the grid connected as shown, a slight grid current is drawn, and the voltage of the point is reduced nearly to 0v; we consider it to be 0v as this is sufficiently accurate for our purpose.

If we consider the effect of a 5% tolerance in the values of the 15K and the two 22K resistors, it turns out that without the grid connected, the voltage at this point, assuming that the cathode of $T_{2,8}$ is +110v, can be as low as -2v and as high as +13v. Hence with the grid connected, no grid current is drawn in the first extreme case, while in the second, about twice the nominal value is drawn. Thus one would expect considerable variation in plate voltage from tube to tube for a 0 input: measured values run from 9v up to 14v with the average of 12.8v. This variability, however, is of no consequence: we will see in our discussion of the Address Dispatch Gates that the plate voltage under discussion must only fall below about 20v for satisfactory operation.

On the other hand, if the $2^0$ stage of $R_3$ contains a 1, the opening of the RIII read out (Green) gate causes a current of 5 ma. to be drawn from the +110v bus, which reduces the voltage of the left grid of $T_{28}$ to +72.5v. The

voltage of the left grid of $T_{3,8}$ accordingly falls to a nominal value of -22v, cutting off the left section of the tube. The actual value is, of course, different from the nominal one for two reasons: cathode rise in $T_{2,8}$ and permitted tolerances in the 15K and the two 22K resistors. Measured values range from -17.5v to -20.3v at the ten grids of $T_{3,8}$, ..., $T_{3,12}$. Actually even -17.5v is about twice the value needed, as we shall see.

We have seen, therefore, that if a 0 is held in the $2^0$ position of $R_3$, the nominal voltage on the corresponding lead (B) is 0v, while if a 1 is held there, the nominal voltage becomes -22v.

Let us now turn our attention to the Recognition Circuit proper. We suppose some "number to be recognized" has been chosen, the voltages representing its digits (0v for 0, -22v for 1) being applied as inputs to the grids of the right-hand sections of $T_{7,7}$, ..., $T_{7,12}$. These inputs are established with the counter in the quiescent state, all outputs (A) representing 0's. We assume that the "number to be recognized" is not 0. Therefore, at least one input (B) is -22v, and this voltage is assumed by at least one of the cathodes of tubes $T_{7,7}$, ..., $T_{7,12}$; hence, at least one section of the 6AL5's $T_{6,8}$, $T_{6,10}$, $T_{6,12}$ is in a conducting state, with plate voltage slightly above -22v, and either the right section of the 2C51, $T_{6,7}$, or one section of the 6J6, $T_{6,11}$, is cut off, with plate voltage, therefore, at +110v. From the tube characteristics it can be seen that for both types used here, with grounded cathodes, 10K plate load resistors, and +110v plate supply voltages, cut off occurs when the grid is dropped slightly below -4v. Thus the -22v available is more than ample, and even -10v would provide an adequate margin of safety. Therefore, either the left section of $T_{6,7}$ is conducting with cathode voltage at +110v or one section of $T_{6,9}$ is conducting with cathode

voltage at +110v; in either case the voltage of the point labelled "Out" in the drawing must be +10v.

Let the counting process now begin. At the count of 1 the cathode of $T_{7,7}$ must follow the left grid to 0v. If the "number to be recognized" is 10000, then all the remaining cathode voltages are already 0v, and with the cathode of $T_{7,7}$ also assuming this value, none of the diodes conduct, all their plate voltages assuming the value 0v. Then the right half of $T_{6,7}$ and both sections of $T_{6,11}$ conduct, their plate voltages falling to about +60v in all cases, which causes the voltage "out" to fall to -27v.

Now consider an arbitrary "number to be recognized". From the previous paragraph it is clear that when the number in the counter reaches agreement with it, the voltage "out" assumes the value -27v. We must still show that the "out" voltage cannot drop to -27v until agreement is reached.

Consider two binary numbers $n > m$; if they are not of the same number of digits, we fill in the missing higher order columns of m with 0's -- this is exactly what occurs in the case under discussion. First we compare the highest order column: n certainly contains a 1 while m may contain a 1 or a 0. If m contains a 1 there, we examine the column of next lower order. Here either both numbers have a 1 or both have a 0, or if there is disagreement, n must have a 1 and m a 0 -- the contrary case is impossible, for then we have $m > n$. Hence, as we move from the highest order columns on down, the first disagreement we meet must always be between a 1 in the larger number and a 0 in the smaller. In columns of lower order than that in which the first disagreement is found, obviously anything can happen.

Physically the last paragraph means that as long as the "number to be recognized" exceeds the number in the True rank of the counter, at least one

of the tubes $T_{7,7}$, ..., $T_{7,12}$ will have its left grid held at -40v and its right grid at -22v, thus assuring a voltage of +10v at "out".

If the counter were permitted to count beyond the "number to be recognized" the voltage "out" could assume either the -27v or the +10v level in different cases, resulting in complete ambiguity. However, there is obviously no trouble here, as there is no point in continuing the count beyond the number to be recognized which will not exceed forty, and the "out" voltage is available to terminate the process, the number of steps in which is being counted, as soon as agreement is reached.

## THE ADDRESS DISPATCH GATES

These are the tubes $T_{4,8}$, ..., $T_{4,12}$ and $T_{5,8}$, ..., $T_{5,12}$ in DWG No. 1289. It has been shown in the discussion of the Recognition Circuit that, for example, of $2^0$ in $R_3$ is 0, the left grid of $T_{5,8}$ assumes a value between +9v and +14v, while if $2^0$ in $R_3$ is 1, this must become +110v. The right-hand grid of $T_{5,8}$ is driven by the left cathode of the 2C51 cathode follower $T_{4,7}$, to the grids of which is applied a voltage of +110v, which is caused to drop to +15v when it is desired to enable the gates. Thus a 0 is signified to the Dispatch Counter by +15v, and a 1 by +110v. The circuit providing the gate command pulse to $T_{4,7}$ had not yet been installed at the time of writing.

## THE GATE-CLEAR SEQUENCING CHAIN

We have seen that the Adder and Digit Resolver form the sum of the contents of $R^3$ (or the complement of this number) and $R_1$ and transmit this sum by way of a set of gates (the Green gates of RI) to $R^1$. As the Green gates transmit 0's, it is necessery first to clear $R^1$ to 1's before opening the gates, so that it is essential that these clear and gate operations should

proceed in the proper time sequence.

The contents of $R^1$ can now be transferred to $R_1$. We recall that the "shift down" operations shift the contents of $R^1$ either one place to the left or one to the right. In each case $R_1$ must be prepared to receive the information transmitted by $R^1$ by the appropriate clearing operation. Thus, for the left shift we clear $R_1$ to 1's and "shift down left" 0's (Green clear and Red gate). while for the right shift we clear $R_1$ to 0's and "shift down right" 1's.

The performance of multiplication and division are facilitated by the structure of the registers. In multiplication the multiplicand is placed in $R^3$ and the multiplier in $R_2$, $R_1$ being cleared to 0. Then if the lowest order digit in $R_2$ (i.e., the contents of $2^{-39}R_2$) is 1, we add the multiplicand to the contents of $R_1$, shift this sum one place to the right, and put it back into $R_1$. We then shift the multiplier one place to the right and repeat the process if the new lowest order digit is a 1, while if it is 0, we merely shift the contents of $R_1$ one place to the right and do the same with that of $R_2$: we are then ready for another step.

Similarly division is performed by a sequence of subtractions and shifts.

Each of these recording and shifting operations requires the following sequence: clear. gate, clear, gate: we refer to such a sequence as a "cycle" of the arithmetic unit, and to a single sequence of clear and gate as a half cycle. For convenience we record the possible operations:

| | |
|---|---|
| Record: | Read Clear, Green Gate |
| Shift up: | Black Clear, Yellow Gate |
| Shift down left: | Green Clear, Red Gate |

Shift down right: Yellow Clear, Black Gate

Obviously the first half cycle is either a "Record" or a "Shift Up", while the second is either "Shift Down Left" or "Shift Down Right".

The proper sequencing of these clearing and gating operations is the function of the "Gate-Clear Sequencing Control", of which a schematic appears in DWG No. 1287. We note that it consists of five main chassis, labelled "CT Bot.", "CG Bot.", etc. For simplicity we number these 1 to 5. Any tube will be referred to as $T_{ij}$ where i signifies the number of the chassis, and j the number attached to that tube in the schematic. There is also a small chassis "CX" containing two dual triodes and a dual diode. Normally the switch in the lead to cathode (1) of $T_{21}$ is set in the position which connects this cathode to cathode (7) of $T_{25}$. The single pole single throw switches in the leads to cathode (7) of $T_{41}$ and to cathode (5) of the diode on chassis "CX" are normally closed.

Inputs to the Sequencing Control are the gate and clear voltages from RI and the Counter Stop voltage, which is that labelled "Out" on the schematic (DWG No. 1289) of the Shift Counter and Recognition Circuit. This voltage has two levels: it remains at +10v until the counter contents agree with the "number to be recognized", at which time it falls to -27v. Outputs are the four voltages shown to the cathodes of the clear selector tubes and the four voltages to the gate driver-drivers in RI and RII.

Thus, it appears that the circuit generates signals which initiate gating and clearing operations, the results of which are fed back to it. One will expect, therefore, that an action once initiated will be self-perpetuating, and this is indeed the case. The Counter Stop signal serves to initiate and to terminate the process, as will be shown.

We first describe in detail the quiescent state of the circuit. Suppose that the gate and clear inputs are all at their upper levels, that the toggles in chassis 1 and 5 have been set in the 1 position (neon lamp glowing), and that the Counter Stop voltage is at its lower level of about -27v; which guarantees that grid (6) of $T_{41}$ is held far below cut-off and consequently that the voltage of plate (1) is high (+110v).

Since the toggle in chassis 1 is in its 1 condition, the voltage of grid (5) of $T_{14}$ is approximately 0v, so that the voltage of plate (2) is slightly less than 50v, while grid (6) is far below cut-off, and hence the voltage of plate (1) is +110v. The plates of $T_{14}$ are connected to the grids of $T_{16}$, both sections of which are connected as cathode followers. From the cathode circuit of the left section, outputs are taken to the grid of the left section of $T_{15}$, and to the grid of the left section of $T_{26}$; similar connections are made from the cathode circuit of the right section to the grid of the right section of $T_{15}$ and that of the left section of $T_{46}$. The voltage divider network from which these outputs are taken are so designed that when the cathode voltage assumes its high value (approximately +110v), a slight grid current is drawn by $T_{15}$ and the grid is held approximately at 0v, and consequently the voltage at the other end of the 1K resistor becomes approximately 7v. On the other hand, when the cathode assumes its low level of voltage, the corresponding section of the $T_{16}$ is cut off, the grid voltage becoming approximately -35v, while that at the other end of the 1K resistor becomes -29v. Now consider the effect on $T_{15}$. Its grid voltages are either -35v or 0v; hence, with a 5.6K plate resistor, the plate voltages are either +110v or approximately +60v. The circuit in chassis 5 is exactly the same and so needs no further discussion.

The outputs of the supertoggle consisting of $T_{41}$ and the tube mounted in the chassis "CX" are very simple: from the cathode (2) of the left section of the latter to the grid (6) of $T_{34}$ and grid (5) of $T_{35}$, and from the cathode (8) of the right section to grid (6) of $T_{36}$ and grid (5) of $T_{35}$. These cathodes can assume two levels: when the toggle holds a 1 the voltage of cathode (2) is approximately +60v and that of cathode (8) is +110v. We assume that the Counter Stop voltage is at its lower level of about -27v, which guarantees that the left half of the Supertoggle tube $T_{41}$ is cut off. We shall see presently that the other section is also held off under these circumstances.

We can now summarize the approximate voltages presented to the remainder of the circuit by the tubes in chassis 1 and 5 and the supertoggle:

| | | | | |
|---|---|---|---|---|
| $T_{26}$ | grid (3):-29v | grid (7):-29v | cathode (2):-29v | cathode (8):-29v |
| $T_{46}$ | grid (3):+7v | grid (7):+7v | cathode (2):+7v | cathode (8):+7v |
| $T_{33}$ | grid (5):+110v | grid (6):+60v | cathode (7):+110v | |
| $T_{34}$ | grid (5):+60v | grid (6):+110v | cathode (7):+110v | |
| $T_{35}$ | grid (5):(see below) | grid (6):+110v | cathode (7):+110v | |
| $T_{36}$ | grid (5):+110v | grid (6):(see below) | cathode (7):+110v | |

These tubes are all cathode followers; in $T_{26}$ and $T_{46}$ the sections are independent, but in each of the rest the cathode is common to both sections, so that the cathode voltage is in each case equal to that of the higher grid. The voltage dividers in the cathode circuits of $T_{33}$, ..., $T_{36}$ are so designed that the output is +8v when one of the grids is high (+110v) and -18v when both grids are low (60v).

We now list the grid voltages of the tubes driven by the cathode followers listed above:

| | | | | |
|---|---|---|---|---|
| | $T_{22}$ | grid (5) +8v | grid (6) +8v | cathode (7) +8v |
| | $T_{23}$ | grid (5) -29v | grid (6) +8v | cathode (7) +8v |
| | $T_{24}$ | grid (5) -29v | grid (6) +8v | cathode (7) +8v |
| II | $T_{25}$ | grid (5) -29v | grid (6) -29v | cathode (7) -29v |
| | $T_{42}$ | grid (5) +8v | grid (6) +8v | cathode (7) +8v |
| | $T_{43}$ | grid (5) +8v | grid (6) +7v | cathode (7) +8v |
| | $T_{44}$ | grid (5) +8v | grid (6) +7v | cathode (7) +8v |
| | $T_{45}$ | grid (5) +7v | grid (6) +7v | cathode (7) +7v |

We also observe that the left section (cathode (1) and plate (7)) of the diode $T_{21}$ is in a conducting state. This holds the grid (5) of $T_{41}$ below cutoff, so that grid (6) of $T_{36}$ and grid (5) of $T_{35}$ are both held at +110v.

The output voltages are now easily obtained:

| | | | | |
|---|---|---|---|---|
| | To $R^1$ Clear Selector | +8v | Red Gate | +8v |
| III | To $R_1$ Clear Selector | +8v | Black Gate | +8v |
| | To $R^2$ Clear Selector | +8v | Green Gate | +8v |
| | To $R_2$ Clear Selector | +8v | Yellow Gate | +8v |

We recall that a positive input to the gate driver drivers disables the gates, while a sufficiently negative one enables them. The disabling voltage of +8v becomes more positive after cathode rises in the cathode followers which serve as gate drivers and gate driver drivers; in practice, the voltages of the -300v, +110v, and +220v buses were all dropped five percent, and the voltage dividers in the cathode circuits of the last four tubes in chassis 3 were then padded until the actual gating voltage was observed to be +10v.

Furthermore, we recall that the clear selector tubes are 6J6's whose grid voltages are the grid voltages of the appropriate toggle, and are thus

either 0v or -40v, while the cathode of the tube is directly connected to the Clear Selector output of the Sequencing Chain. With this cathode held at +8v, obviously both sections of the Clear Selector tube are cut off, and the clear bus voltage is held at +150v, while when the cathode is dropped midway between 0v and -40v, the section whose grid is at 0v conducts, while the other remains cut off.

Hence, the condition of the Sequencing Chain described above is a stable one: no clears or gates are generated and hence none are fed back to change the condition of the Sequencing Chain circuitry.

Now let the Counter Stop voltage be raised from -27v to +10v. This permits grid (6) of $T_{41}$ to rise in voltage to 0v, beyond which it cannot go (more than a few tenths of a volt) because of the grid current that starts to flow. Thus, the supertoggle is put in the 1 condition and the voltage of cathode (2) of the supertoggle cathode follower falls to +60v, which brings the voltages of grid (6) of $T_{34}$ and grid (5) of $T_{33}$ both down to +60v. Referring to table I it is clear that this action causes the cathode voltages of these two tubes also to fall to +60v, and hence grids (5) of $T_{42}$ and $T_{44}$, grid (6) of $T_{42}$, and grid (5) of $T_{43}$ all fall from +8v to -18v. Reference to table II now shows that the cathode voltage of $T_{42}$ falls to -18v, but those of $T_{43}$ and $T_{44}$ are both caught at +7v by the other grids of those tubes. Thus the net effect so far of the rise in the Counter Stop voltage is to cause the $R^1$ and $R^2$ Clear Selector voltages to fall to -18v: we need only concern ourselves with the clearing of $R^1$, as it is this voltage which is fed back to the Sequencing Control.

Thus we have:

| | | | | | |
|---|---|---|---|---|---|
| I' | $T_{26}$ | grid (3):-29v | grid (7):-29v | cathode (2):-29v | cathode (8):-29v |
| | $T_{46}$ | grid (3):+7v | grid (7):+7v | cathode (2):+7v | cathode (8):+7v |
| | $T_{33}$ | grid (5):+60v | grid (6):+60v | cathode (7):+60v | |
| | $T_{34}$ | grid (5):+60v | grid (6):+60v | cathode (7):+60v | |
| | $T_{35}$ | grid (5):+110v | grid (6):+110v | cathode (7):+110v | |
| | $T_{36}$ | grid (5):+110v | grid (6):+110v | cathode (7):+110v | |

whence

| | | | | |
|---|---|---|---|---|
| II' | $T_{22}$ | grid (5):+8v | grid (6):+8v | cathode (7):+8v |
| | $T_{23}$ | grid (5):-29v | grid (6):+8v | cathode (7):+8v |
| | $T_{24}$ | grid (5):-29v | grid (6):+8v | cathode (7):+8v |
| | $T_{25}$ | grid (5):-29v | grid (6):-29v | cathode (7):-29v |
| | $T_{42}$ | grid (5):-18v | grid (6):-18v | cathode (7):-18v |
| | $T_{43}$ | grid (5):-18v | grid (6):+7v | cathode (7):+7v |
| | $T_{44}$ | grid (5):-18v | grid (6):+7v | cathode (7):+7v |
| | $T_{45}$ | grid (5):+7v | grid (6):+7v | cathode (7):+7v |

and the outputs become:

| | | | | |
|---|---|---|---|---|
| III' | To $R^1$ Clear Selector | -18v | Red Gate: | +8v |
| | To $R_1$ Clear Selector | +8v | Black Gate: | +8v |
| | To $R^2$ Clear Selector | -18v | Green Gate: | +7v |
| | To $R_2$ Clear Selector | +8v | Yellow Gate | +7v |

Whether the Red Clear ($R^1$ to 1) or the Black Clear ($R^1$ to 0) takes place now depends upon whether $2^{-39}R_2$ holds a 1 or a 0, but obviously one of these must occur. Suppose, for example, that the Black Clear occurs, the voltage of the Black Clear bus falling from +150v to +50v. Evidently this

also clears the toggle in Chassis 1 to 0, and we must trace the consequences of this event. It is easiest to show these by another series of tables:

| | | | | | |
|---|---|---|---|---|---|
| | $T_{26}$ | grid (3):+7v | grid (7):-29v | cathode (2):+7v | cathode (8):-29v |
| | $T_{46}$ | grid (3):+7v | grid (7):-29v | cathode (2):+7v | cathode (8):-29v |
| I" | $T_{33}$ | grid (5):+60v | grid (6):+60v | cathode (7):+60v | |
| | $T_{34}$ | grid (5):+110v | grid (6):+110v | cathode (7):+110v | |
| | $T_{35}$ | grid (5):+110v | grid (6):+110v | cathode (7):+110v | |
| | $T_{36}$ | grid (5):+60v | grid (6):+110v | cathode (7):+110v | |

These changes in turn influence the tubes in chassis 2 and 4 as follows:

| | | | | |
|---|---|---|---|---|
| | $T_{22}$ | grid (5):+8v | grid (6):+8v | cathode (7):+8v |
| | $T_{23}$ | grid (5):+7v | grid (6):+8v | cathode (7):+8v |
| | $T_{24}$ | grid (5):-29v | grid (6):+8v | cathode (7):+8v |
| II" | $T_{25}$ | grid (5):+7v | grid (6):-29v | cathode (7):+7v |
| | $T_{42}$ | grid (5):+8v | grid (6):-18v | cathode (7):+8v |
| | $T_{43}$ | grid (5):-18v | grid (6):-29v | cathode (7):-18v |
| | $T_{44}$ | grid (5):+8v | grid (6):+7v | cathode (7):+8v |
| | $T_{45}$ | grid (5):+7v | grid (6):-29v | cathode (7):+7v |

Thus we have:

| | | | | |
|---|---|---|---|---|
| | To $R^1$ Clear Selector: | +8v | Red Gate: | +8v |
| III" | To $R_1$ Clear Selector: | +8v | Black Gate: | +8v |
| | To $R^2$ Clear Selector: | +8v | Green Gate: | +8v |
| | To $R_2$ Clear Selector: | +8v | Yellow Gate: | -18v |

Thus the Black Clear is terminated and the Yellow Gate enabled. Lags through the circuits cause an interval of 1.5 μsec. to elaspse between the initiation and termination of the Black Clear.

The Yellow Gate which is now enabled is fed back to the Sequence Control: the voltage of grid (6) of $T_{51}$ drops to about -20v and enables the other section to draw plate current: this is, of course, the standard gating procedure for reading into a toggle, and the toggle in chassis (5) is caused to flip to its 0 state. It is now necessary to trace the consequences of this, which we do again by listing the voltages throughout the circuit.

I"'

| | | | | |
|---|---|---|---|---|
| $T_{26}$ | grid (3):+7v | grid (7):+7v | cathode (2):+7v | cathode (8):+7v |
| $T_{46}$ | grid (3):-29v | grid (7):-29v | cathode (2):-29v | cathode (8):-29v |
| $T_{33}$ | grid (5):+60v | grid (6):+110v | cathode (7):+110v | |
| $T_{34}$ | grid (5):+110v | grid (6):+60v | cathode (7):+110v | |
| $T_{35}$ | grid (5):+110v | grid (6):+60v | cathode (7):+110v | |
| $T_{36}$ | grid (5):+60v | grid (6):+110v | cathode (7):+110v | |

Thus the voltages in chassis 2 and 4 are:

II"'

| | | | |
|---|---|---|---|
| $T_{22}$ | grid (5):+8v | grid (6):+8v | cathode (7):+8v |
| $T_{23}$ | grid (5):+7v | grid (6):+8v | cathode (7):+8v |
| $T_{24}$ | grid (5):+7v | grid (6):+8v | cathode (7):+8v |
| $T_{25}$ | grid (5):+7v | grid (6):+7v | cathode (7):+7v |
| $T_{42}$ | grid (5):+8v | grid (6):+8v | cathode (7):+8v |
| $T_{43}$ | grid (5):+8v | grid (6):-29v | cathode (7):+8v |
| $T_{44}$ | grid (5):+8v | grid (6):-29v | cathode (7):+8v |
| $T_{45}$ | grid (5):-29v | grid (6):-29v | cathode (7):-29v |

And so we have

III"'

| | | | |
|---|---|---|---|
| To $R^1$ Clear Selector: | +8v | Red Gate: | +8v |
| To $R_1$ Clear Selector: | +8v | Black Gate: | +8v |

| | | | | |
|---|---|---|---|---|
| III"' | To $R^2$ Clear Selector: | +8v | Green Gate: | +8v |
| | To $R_2$ Clear Selector: | +8v | Yellow Gate: | +8v |

so that the Yellow Gate has been disabled. Again, due to delays in the circuitry, the disabling of the Yellow gate occurs about 1.5 μsec. after its enabling. Another effect is that since the cathode voltage of $T_{45}$ falls to -29v, conduction takes place in the left section of the CX diode and in the right section of diode $T_{21}$, which causes the grid (6) of supertoggle tube $T_{41}$ to fall below cut off. As cathode (1) of $T_{21}$ is held at +7v, there is nothing to prevent the flipping of the supertoggle which accordingly assumes its 0 condition. This in turn raises the voltages of grid (6) of $T_{34}$ and grid (5) of $T_{33}$ to +110v, and lowers those of grid (6) of $T_{36}$ and grid (5) of $T_{35}$ to +60v: thus

| | | | | |
|---|---|---|---|---|
| $T_{26}$ | grid (3):+7v | grid (7):+7v | cathode (2):+7v | cathode (8):+7v |
| $T_{46}$ | grid (3):-29v | grid (7):-29v | cathode (2):-29v | cathode (8):-29v |
| $T_{33}$ | grid (5):+110v | grid (6):+110v | cathode (7):+110v | |
| $T_{34}$ | grid (5):+110v | grid (6):+110v | cathode (7):+110v | |
| $T_{35}$ | grid (5):+60v | grid (6):+60v | cathode (7):+60v | |
| $T_{36}$ | grid (5):+60v | grid (6):+60v | cathode (7):+60v | |

and

| | | | | |
|---|---|---|---|---|
| | $T_{22}$ | grid (5):-18v | grid (6):-18v | cathode (7):-18v |
| | $T_{23}$ | grid (5):+7v | grid (6):-18v | cathode (7):+7v |
| II"" | $T_{24}$ | grid (5):+7v | grid (6):-18v | cathode (7):+7v |
| | $T_{25}$ | grid (5):+7v | grid (6):+7v | cathode (7):+7v |
| | $T_{42}$ | grid (5):+8v | grid (6):+8v | cathode (7):+8v |
| | $T_{43}$ | grid (5):+8v | grid (6):-29v | cathode (7):+8v |

| | | | | |
|---|---|---|---|---|
| II"" | $T_{44}$ | grid (5):+8v | grid (6):-29v | cathode (7):+8v |
| | $T_{45}$ | grid (5):-29v | grid (6):-29v | cathode (7):-29v |

the output voltages becoming:

| | | | | |
|---|---|---|---|---|
| III"" | To $R^1$ Clear Selector: | +8v | Red Gate: | +7v |
| | To $R_1$ Clear Selector: | -18v | Black Gate: | +7v |
| | To $R^2$ Clear Selector: | +8v | Green Gate: | +8v |
| | To $R_2$ Clear Selector: | -18v | Yellow Gate: | +8v |

Hence, a Yellow or Green Clear is made possible: which is to be performed is determined by the $R_1$ Clear Selector, which is controlled by the "multiply/divide" toggle. We also observe that the state of the supertoggle remains unchanged, since the cathode voltages of $T_{25}$ and $T_{45}$ do not change.

We have traced in detail one half cycle of operation of the sequencing chain. We began with the toggles in chassis 1 and 5 cleared to 1, the Counter Stop voltage low, and consequently both sections of the supertoggle tube cut off. This was a stable state of the circuit, which in this condition permitted no gating or clearing operations to be performed. When the Counter Stop voltage was raised to its higher value, the supertoggle assumed its 1 condition. This dropped the voltage output to the $R^1$ and $R^2$ Clear Selector, which decided, on the basis of the contents of $2^{-39}R_2$, whether to perform a Black or Red Clear. We assumed that the Black Clear was called for. The Black Clear being fed back to the Sequencing Chain flipped the toggle in chassis (1) to 0 which had two consequences: 1) the Black Clear was terminated, and 2) a Yellow Gate was enabled. Again the feeding back of the Yellow Gate signal flipped the toggle in chassis (5) to 0. This action had again two consequences: 1) the Yellow Gate was terminated, and 2) the supertoggle was

flipped to 0. This in turn permitted the performance of a Yellow or Green Clear, depending upon the state of the Multiply/Divide toggle.

If the Red Clear had been called for, the sequence would have been: flip the toggle in chassis (5) to 0, terminate the Clear, enable the Green Gate, flip the toggle in chassis (1) to 0, disable the Green Gate, flip the supertoggle to 0.

By continuing the process, we find that, providing the Yellow Clear was called for, the signal fed back to the Sequencing Chain flips the toggle in chassis (1) to 1 which terminates the Clear and enables the Black Gate. This in turn being fed back flips the toggle in chassis (5) to 1 disables the Black Gate, and flips the supertoggle again to 1. If the Green Clear is called for, the toggle in chassis (5) is first flipped to 1, the clear terminated and the Red Gate enabled. This in turn is fed back to flip the toggle in chassis (1) to 1, disable the gate, and finally to flip the supertoggle back to 1.

Thus beginning with all three toggles in the 1 condition, first a Red or Black Clear is performed followed by a Green or a Yellow Gate, respectively, at the end of which all the toggles are in the 0 condition: this is one half cycle. The second half cycle begins with a Yellow or Green Clear, depending upon the arithmetical process to be performed. These are respectively followed by Black or Red Gates, at the termination of which all the toggles are again in the 1 condition, and the circuit is ready for another cycle of operation.

## THE DISPATCH COUNTER

The operation of the Williams Memory requires the periodic regeneration of the information stored therein. The practical upper bound on the time

between regenerations is about one-tenth of a second; actually it is desirable to make this interval shorter, one-thirtieth of a second being satisfactory. The CRT beams must, therefore, be directed in this interval to each of the memory locations. This requires that in the interval all possible memory addresses must be generated and presented to the deflection circuits. Each memory address is specified by a ten binary digit number, one group of five digits specifying the horizontal coordinate; the remaining five the vertical coordinate. Hence, a ten stage binary counter which starts at 0 and counts until all the stages hold 1's will generate in the process all memory locations just once.

Furthermore, using as we do a one-address code, we store orders in successive locations in the memory and use them in the order in which they are stored. There is, however, an exception to this in the case where it becomes necessary to shift control, as for example, when it is desired to repeat a sequence of instructions using new values of the numerical quantities.

It appears at first glance that the requirements of the Williams Memory which have been stated above require two counters. However, these can be combined into a single device which we call the Dispatch Counter. This is a double counter of the Adder type, consisting physically of three ranks of ten toggles each and the necessary gate, clear, and carry circuits. Each count which arrives at the input causes unity to be added to the lowest order ($2^0$) stage and carries to be propagated as appropriate to the higher order stages.

The three ranks of toggles are referred to as the "restore", "dispatch", and "order" toggles ($T_R$, $T_D$, $T_O$): the $T_D$ and $T_R$ toggles form the counter

which generates the memory addresses for the regeneration process, while the $T_O$ and $T_D$ toggles form the order counter. Leads directly out of the stages of $T_D$ are taken to the Williams Memory Deflection Generator, while leads into $T_D$ make it possible, when it is desired to "shift control", to replace the contents of $T_D$ by an arbitrary number. Inputs are pulses generated in the Williams Memory Local Control: according as a Regenerate or an Action cycle is to take place, these are caused to increase the number in $T_R$ or $T_O$ by unity.

The schematic of the Dispatch Counter is shown in DWG No. 1336:two typical stages are drawn at the left, while the tubes at the right and in the upper left corner are gate drivers.

Consider a typical stage of the Counter. The convention here is that a toggle holds 1 when the left section conducts, as can be seen by the arrangement of the neon lamps. The tube (2C51) directly above $T_D$ provides the gates between $T_D$ and $T_R$, the left section being the $B_R$ or "down" gate and the right section the $A_R$ or "up" gate; the 2C51 directly below $T_D$ provides the gates between $T_D$ and $T_O$, the left section being the $A_O$ or "down" gate and the right the $B_O$ or "up" gate. Observe that the $B_R$ gate guarantees that $T_D$ will hold the same bit as $T_R$, while clearing $T_D$ to 1's followed by enabling the $B_O$ gate guarantees that $T_D$ will hold the same bit as $T_O$. The operation of the A gates will be explained later. The grid voltages of $T_D$ drive cathode followers; these are both sections of a 2C51. From the cathode of the left hand section an output is taken to the deflection gates in the Williams Memory; from each section an output is tapped down slightly below the cathode. We may assume that the values of these voltages are 0v and -40v for the two states of $T_D$. The 6J6 directly above $T_O$ will be referred

to as the carry gate, while the function of the double diode will be explained below.

The "dispatch" rank of toggles operates together with either the "restore" or the "order" rank as a true adder. Suppose the number held in the "restore" rank is to be increased by unity. The first step is to clear the "dispatch" rank to 0, then to open the $B_R$ gates. This puts into $T_D$ the number held in $T_R$. To this number 1 is added automatically by introducing a permanently wired in carry to the lowest order stage. This does not change the state of the $T_D$ toggles, but sets up the voltages on the grids of the $A_R$ gates in such a way that when subsequently $T_R$ is cleared to 1's and the A gates opened, $T_R$ receives a number greater by unity than the one previously held.

As we saw in studying the Williams Memory local control, the decision as to whether the next memory cycle is to be one of action or regeneration is made during the $\bar{A}$ pulse. This decision determines whether unity is to be added to the contents of $T_R$ or $T_O$. The next pulse, "Cl", then performs the proper clearing operation in $T_D$ (the "B clear"), then B is used to open the B gates. At the beginning of the next cycle, "Cl $T_1$" clears $T_R$ (or $T_O$ as the case may be) while a pulse coinciding in time with $T_D$ opens the A gates.

Suppose that unity is to be added to the contents of $T_R$: then this number is read into $T_D$ by the $B_R$ gates, and we wish to see how the addition of unity is effected.

In each stage of $T_D$ we can have either a 1 or a 0 held in the toggle (the Resident Digit), and either a 1 or a 0 as the carry out. This gives us four cases as shown in the table. In each case we also show the carry from the preceeding stage, the carry which must be passed on to the next stage,

the Resident Digit ($D_R$), and the "new" Resident Digit ($D_R'$):

| | C in | $D_R$ | C out | $D_R'$ |
|---|---|---|---|---|
| I | 0 | 0 | 0 | 0 |
| II | 0 | 1 | 0 | 1 |
| III | 1 | 0 | 0 | 1 |
| IV | 1 | 1 | 1 | 0 |

As we said before, the "carry" input to the lowest order stage is permanently wired to a point of negative voltage (-300v), which is the means used to introduce a 1 into the first stage in the form of an artificial carry. A carry of 1 is always given by a negative voltage, while a 0 carry is signified by a positive voltage. In the actual circuit, the lowest observed 0 carry voltage was +5v, the highest +26v, while the 1 carry voltages ranged from -23v to -27v.

We will now consider in detail each of the four cases for an arbitrary stage: of course, only cases III and IV can occur in the first stage.

I. The voltage of the right grid of the carry gate is -40v, while that of the left grid is positive. The cathode, therefore, follows the left grid high enough to cut off the right section, causing a positive (0) carry to be transmitted to the next stage. If all the resistors in the plate network of the right section of the carry gate had exactly their nominal values, this carry voltage would be +21.4v; the effect of tolerances is such that values of from +5v to +26v were observed in the ten stages of the counter, as noted above. The grid of the $A_R$ gate would go far negative, but it is held up by conduction through the left section of the dual diode to about 0v; measured values of from 0v to +1v were observed.

Next, the $T_R$ toggle is cleared to 1, and subsequently the $A_R$ gate is opened by dropping the cathode voltage to -10v. As the grid voltage of the $A_R$ gate tube is 0v, conduction takes place which flips the $T_R$ toggle back to 0. Hence, $D_R' = D_R = 0$ and C out = 0.

II. Though here the right grid of the carry gate attains a voltage of 0v, the cathode is still held up sufficiently by the positive voltage of the left grid that the right section is cut off. Again the carry to the next stage is a positive voltage. The left plate of the dual diode is now connected to a point below ground, while the cathode of the right section is positive. Hence, the diode is inoperative, and the grid of the $A_R$ gate becomes quite negative -- from -28v to -31v in the ten stages of the counter.

This suffices to prevent the enabling signal to the $A_R$ gate from having any effect, and, therefore, the $T_R$ toggle, once cleared to 1, will remain in that condition. Hence, $D_R' = 1$ and C out = 0.

III. Both grids of the carry gate are negative. We have mentioned that the highest value of voltage observed for a carry of 1 is -23v. The right grid of the $T_D$ toggle is high (0v) which permits both diode sections to conduct, and thus to hold the carry gate cathode voltage so high that both sections are cut off. Hence, we obtain a positive carry voltage to the next stage, while the $A_R$ gate grid voltage is observed to lie between -10v and -12v.

Thus when the $A_R$ gate is enabled, it does not draw sufficient current to flip the $T_R$ toggle from 1, to which it has been cleared, back to 0. Hence, $D_R' = 1$, C out = 0.

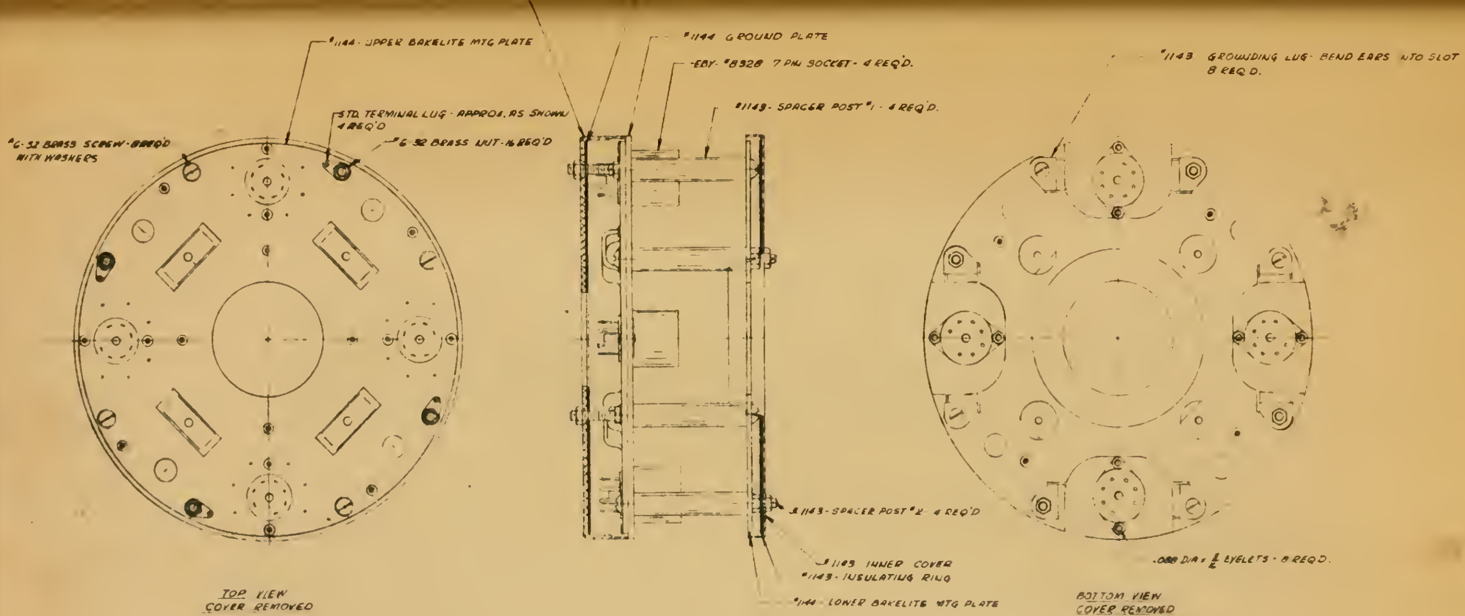
IV. Here the cathode of the carry gate follows the right grid high enough to cut off the left section, giving a negative (1) carry to the next

stage. The grid of the $A_R$ gate is prevented from going positive by conduction through the right section of the diode: observed values of grid voltage range from 0v to -1.5v.

Hence when the $A_R$ gate is enabled, sufficient current is drawn to flip $T_R$ back to 0, and we have $D_R' = 0$, C out = 1.

Thus, in the two cases (II and III) in which the "new" digit in the stage under consideration, resulting from the addition of the carry from the previous stage to the resident digit, is a 1, the $A_R$ gate grid voltage is always less than -10v, while in the two cases (I and IV) in which it is a 0, the $A_R$ gate grid voltage lies in the range from -1.5v to +1v. Thus we see why it is necessary to clear $T_R$ to 1's before opening the $A_R$ gates; furthermore, it is clear that the $A_R$ gates are kept closed as long as the cathode voltage is +10v, which is a convenient level obtained from the Williams Memory Local Control. The opening of the gates can be accomplished by dropping the cathode below the +1v, -1.5v range. Faster action is obtained the lower the cathode is dropped, but it is necessary to keep this level sufficiently high that a grid voltage of -10v will not result in the drawing of sufficient current to flip the $T_R$ toggle: a lower value of -6v instead of -10v would appear to be reasonable here.

This suffices to illustrate the operation of the Dispatch Counter. A complete account of its functioning in the system must await the completion of the Main Control.



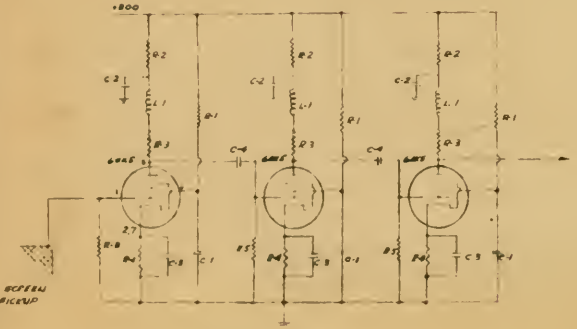
TOP VIEW
COVER REMOVED

BOTTOM VIEW
COVER REMOVED

ELECTRICAL PARTS LIST

| NO. | PART | TYPE | VALUE | RATING | MFGR |
|---|---|---|---|---|---|
| R-1 | RESISTOR | CARBON | 9.1K | 1W | – |
| R 2 | " | " | 27K | 2W | – |
| R 3 | " | " | 6.8K | 1W | – |
| R-4 | " | " | 330 Ω | 1W | – |
| R 5 | " | " | 100K | 1W | – |
| C-1 | CONDENSER | PAPER * | .01µf | 400V D.C | AEROVOX |
| C 2 | " | PAPER * | .1µf | 600V DC | SPRAGUE |
| C 3 | " | PAPER * | 25µf | 400V D.C | GEN'L #8351207-B OR MCARNOLD EQUIV. |
| C 4 | " | MICA | 1000µµf | · | M'CARNOLD |
| L-1 | CHOKE | | 50µh | | |

* TUBULAR METAL TYPE · ONE SIDE GD.

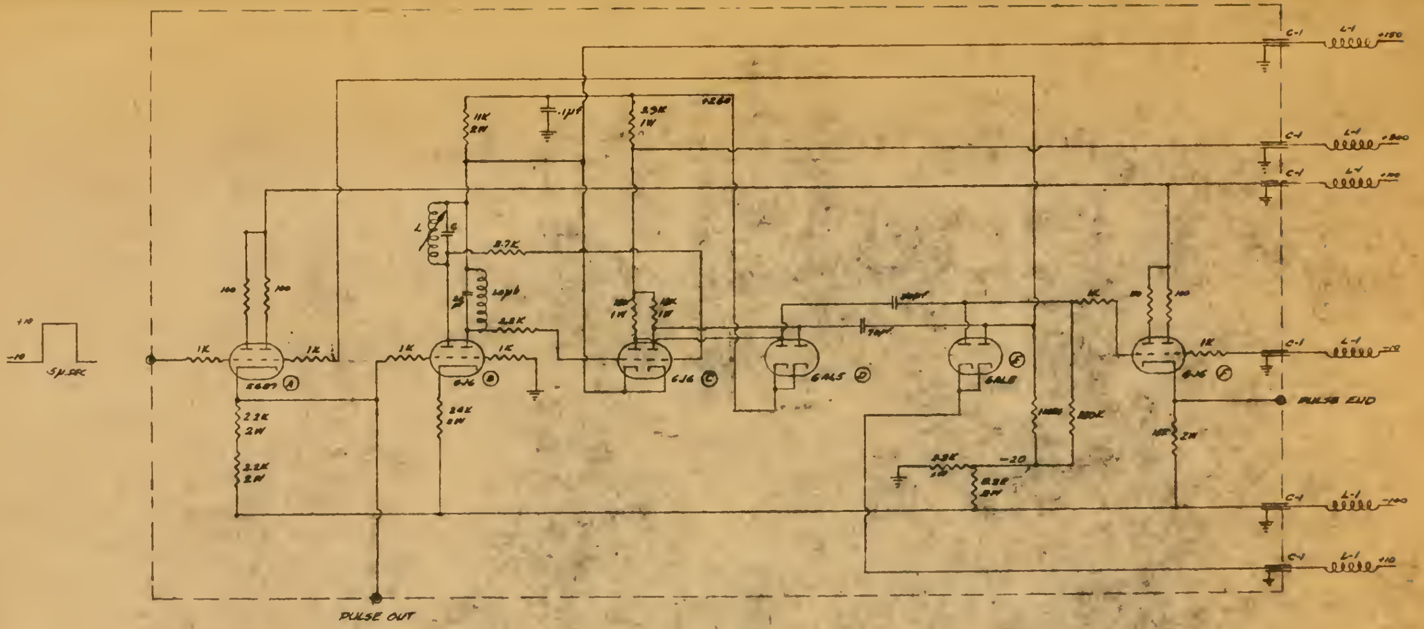


AMPLIFIER SCHEMATIC

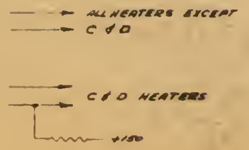
ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.

AMPLIFIER ASSEMBLY
WILLIAMS MEMORY RACK

DRAWN: EMSLIE | DATE: DEC 16 1949
SCALE: FULL | DWG. No. 1142



L-1 - MILLER #692 30μH CHOKE
C-1 - SPRAGUE .1μf BYPASS CAPACITOR



| RANGE | L-(MIN) | C |
|---|---|---|
| 0.75-1.5 μs | 1.42 μh | 20 μμf |
| 1-2 μs | 2.02 μh | 30 μμf |
| 1.5-3 μs | 3.04 μh | 55 μμf |
| 2-4 μs | 4.05 μh | 80 μμf |

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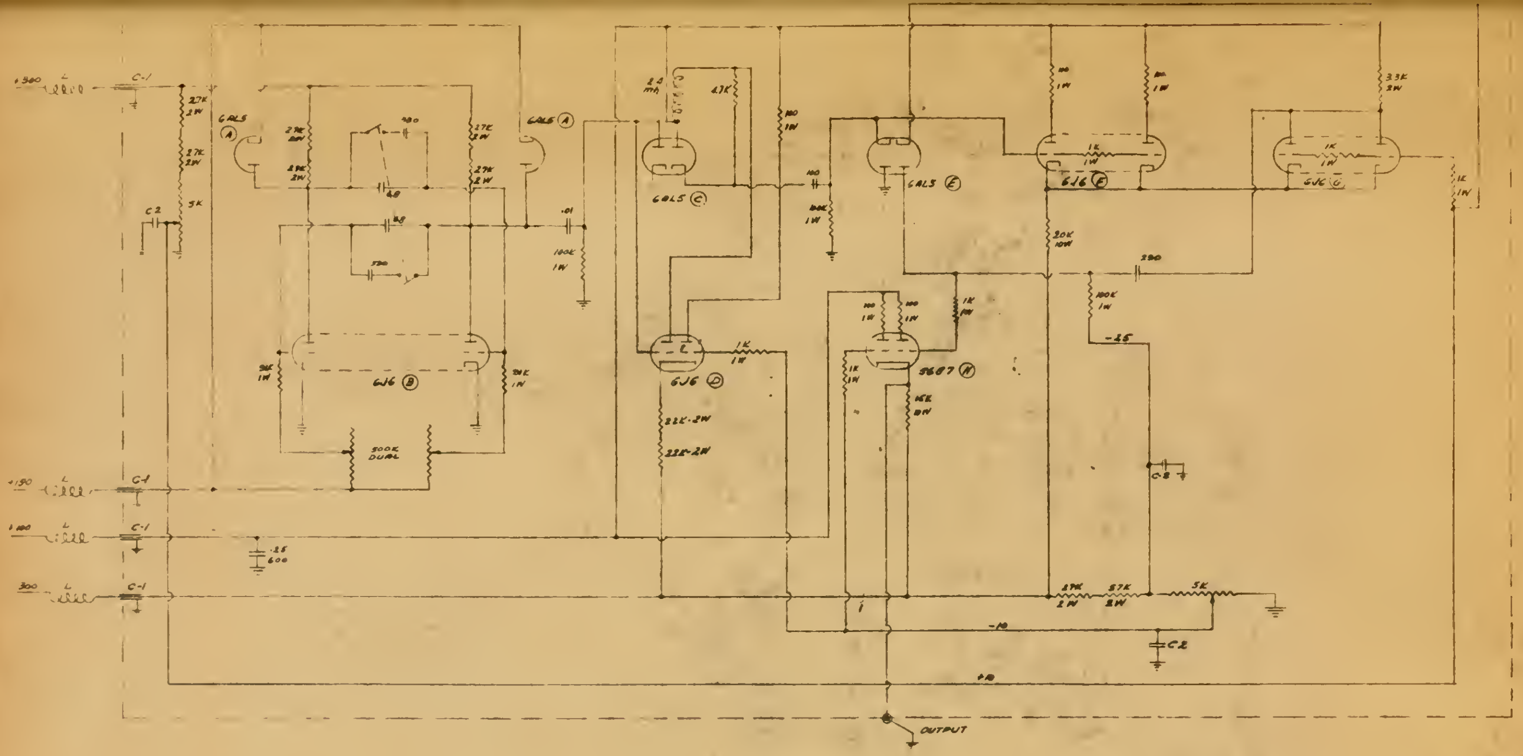
W.D. - WILLIAMS TUBE PULSER

DRAWN: EMSLIE
DATE: JUNE 13 1950
SCALE:
DWG. No. 1216



RANGES -
7-38µS(143-26 KC)
35-240µS (28-4 KC)

L - MILLER #692 30MA CHOKE

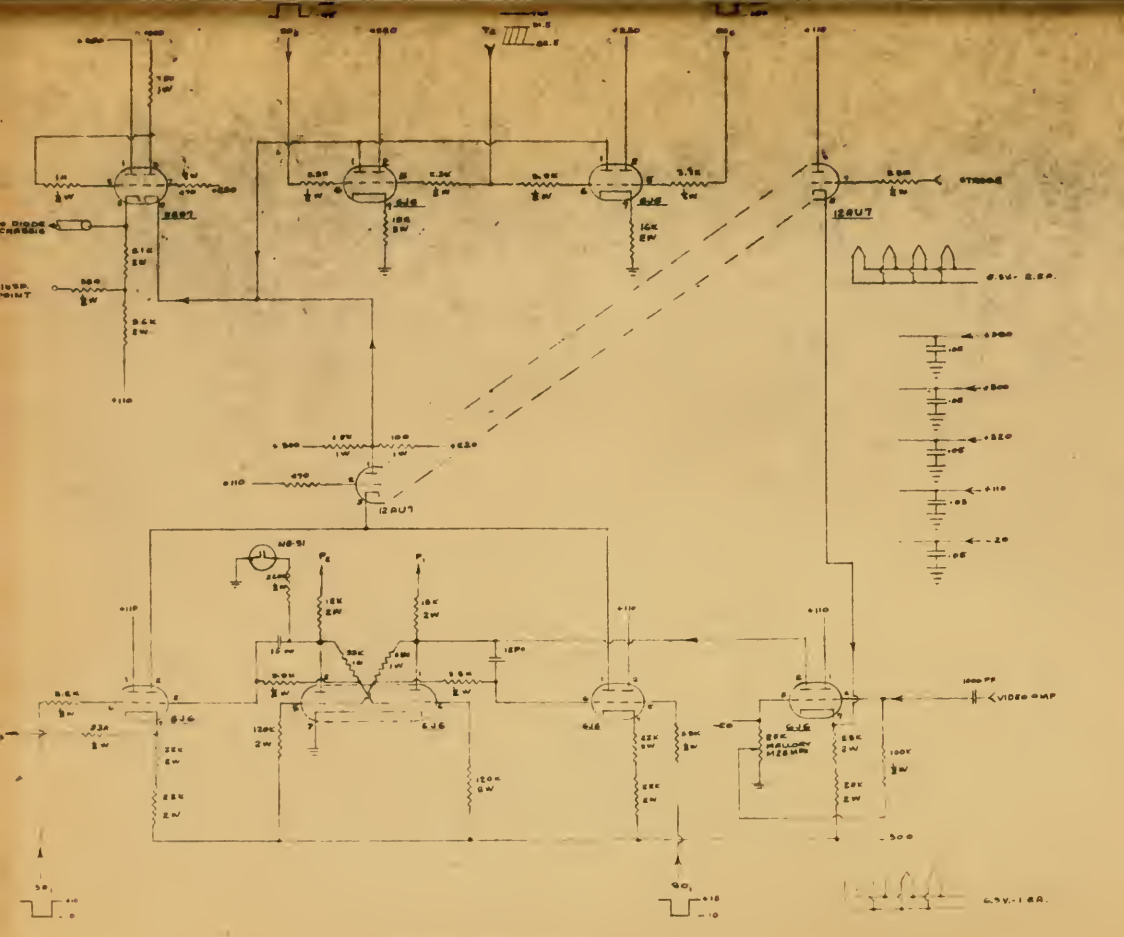
C-1 SPRAGUE 0.1µF, 600V BYPASS CAP.

C-2 3×.1µF - 600V.

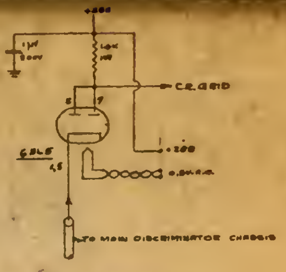
**ELECTRONIC COMPUTER PROJECT**
**INSTITUTE FOR ADVANCED STUDY**
PRINCETON, N. J.

MEMORY CLOCK-II
REVISION #1

DRAWN. EMSLIE
DATE: JUNE 14, 1950
SCALE:
DWG. No.1217



MAIN DISCRIMINATOR SCHEMATIC



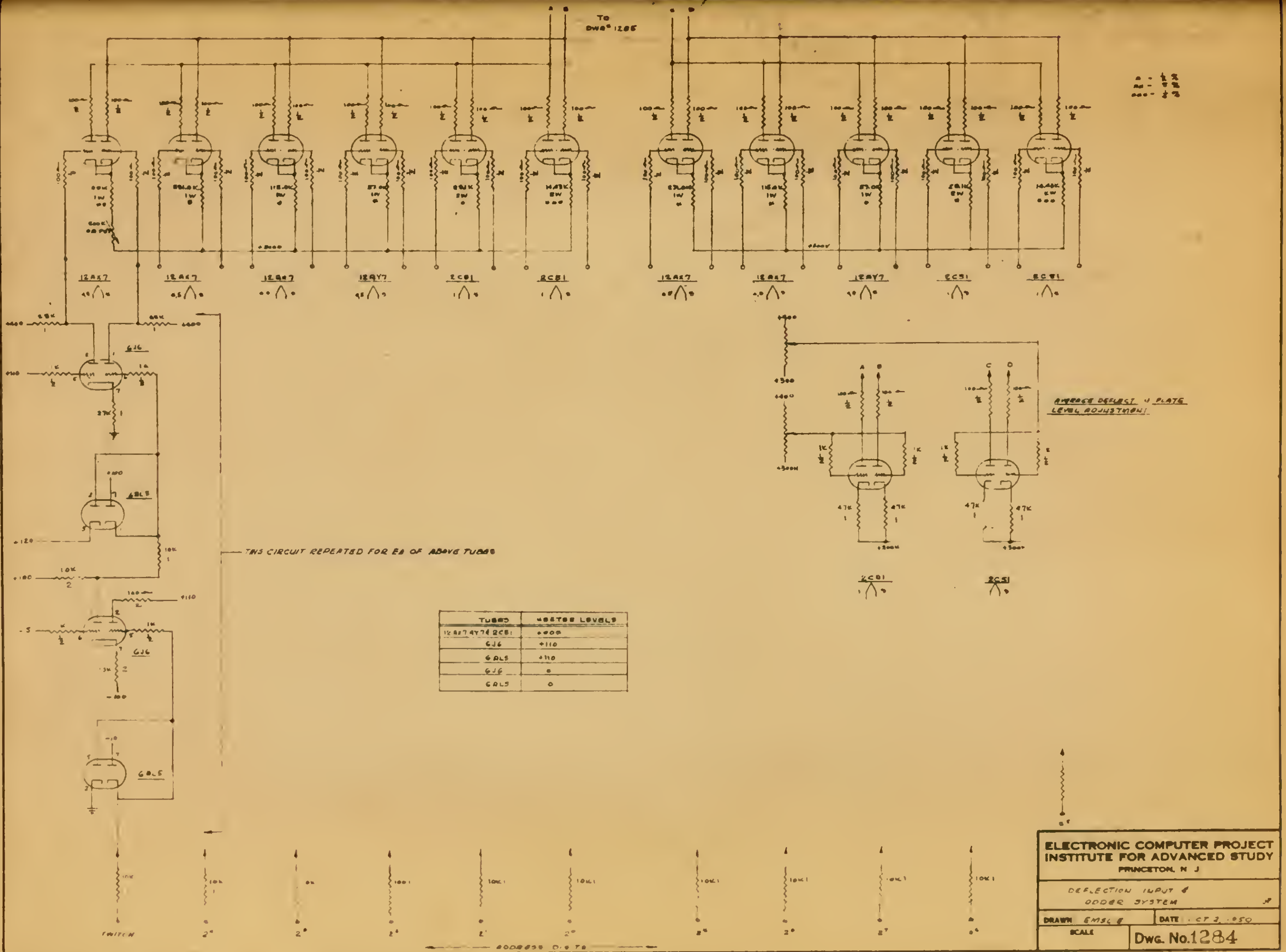
DIODE CHASSIS SCHEMATIC
(SINGLE SOCKET CHASSIS #1896)

| D.C.VOLTS | PULSES | HEATERS |
|---|---|---|
| +300 | SO₁ | 6.3V-1.8A  0 V DC. |
| +200 | SA₁ | 6.3V-2.2A |
| +220 | SO₂ | |
| +110 | SA₂ | INPUT - AMP. |
| 0 | STROBE | OUTPUTS - C R GRID |
| -20 | P₁ (+150) | SLAVE |
| -300 | P₂ (+150) | |

ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.

DISCRIMINATOR WIRING LAYOUT
NMS MEMORY RACK

DRAWN: EMSLIE  DATE JULY 26, 1950
SCALE —  DWG. No. 1241



| TUBES | HEATER LEVELS |
|---|---|
| 12AX7 AY7 & 2C51 | +300 |
| 6J6 | +110 |
| 6AL5 | +110 |
| 6J6 | 0 |
| 6AL5 | 0 |

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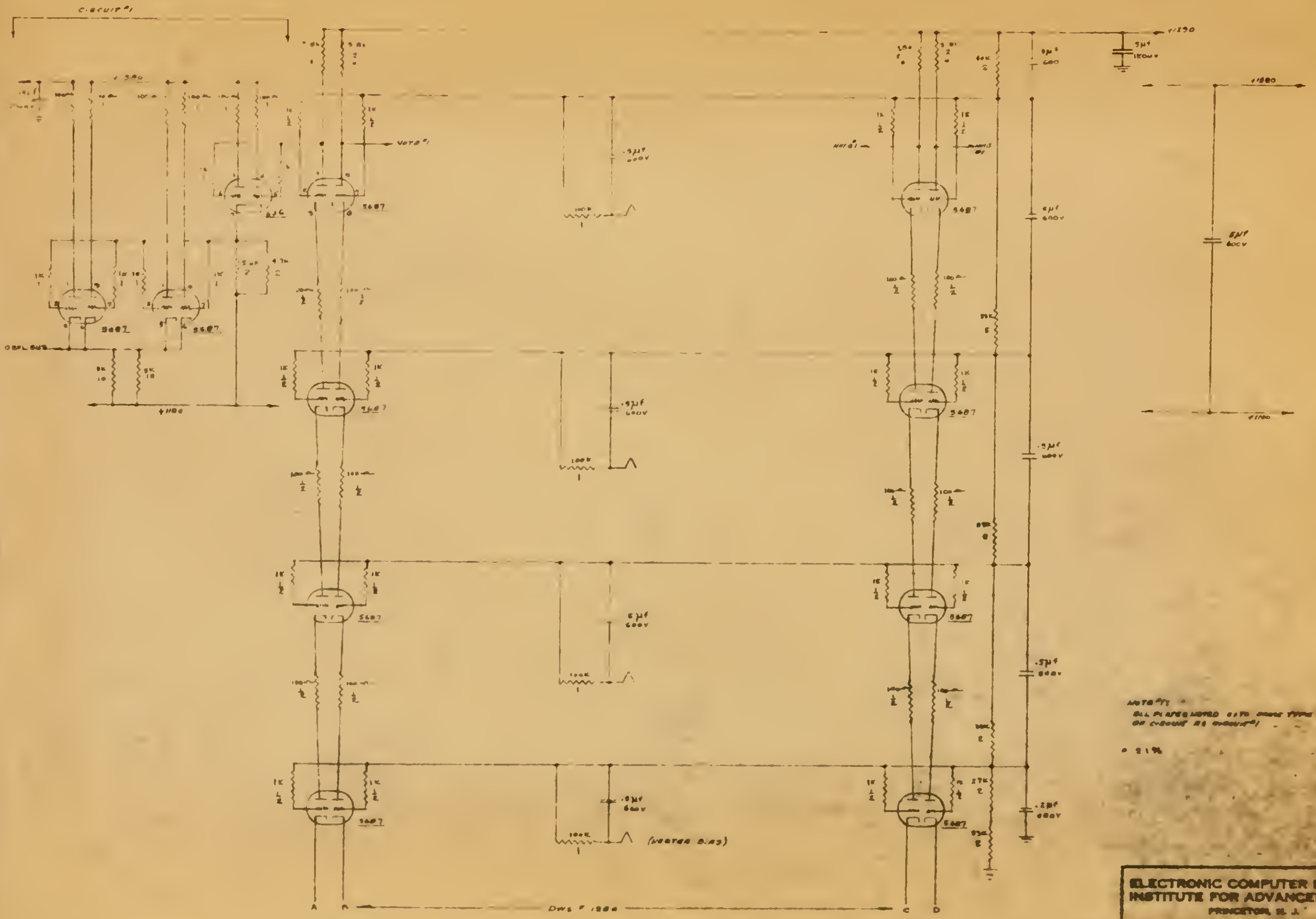
DEFLECTION INPUT &
ADDER SYSTEM

DRAWN EMSL E
DATE OCT 2, 1950
SCALE
Dwg. No.1284

D. & W. Blue Print Co.



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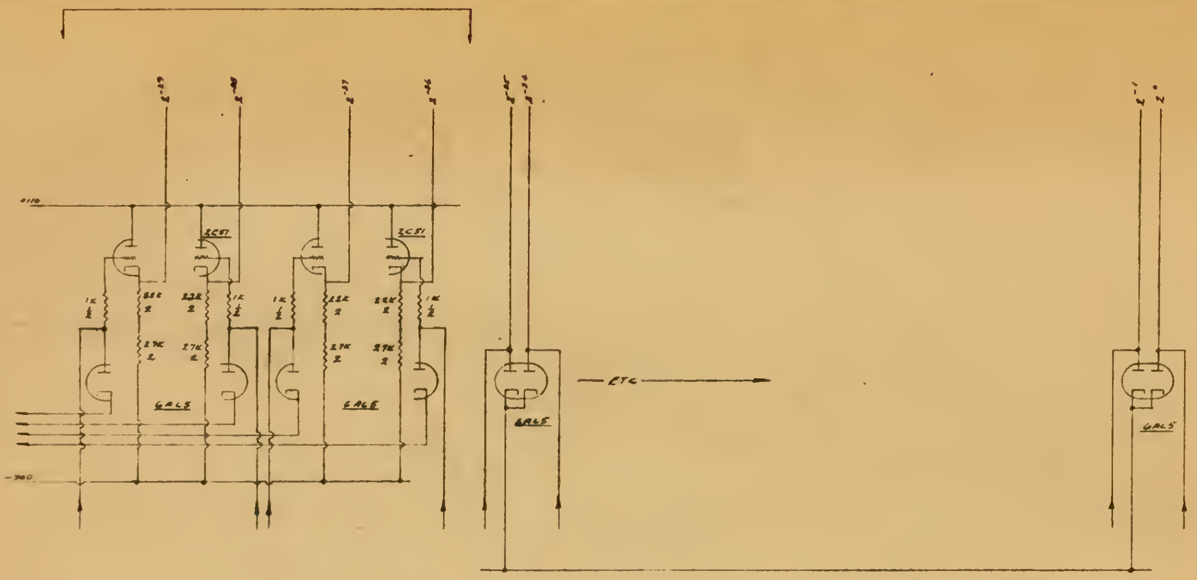
DEFLECTION DRIVER SYSTEM

DRAWN: EMSLIE
DATE: OCT 6, 1950
SCALE:
Dwg. No. 1285

MODIFICATION OF LAST FOUR STAGES FOR
TELETYPE READ-IN



HEATER BIAS - ALL 6AL5'S +150V FROM A20 (DWG #1263)
ALL 2C51'S = 0V.

FOR CHASSIS SEE DWG #1265

**ELECTRONIC COMPUTER PROJECT**
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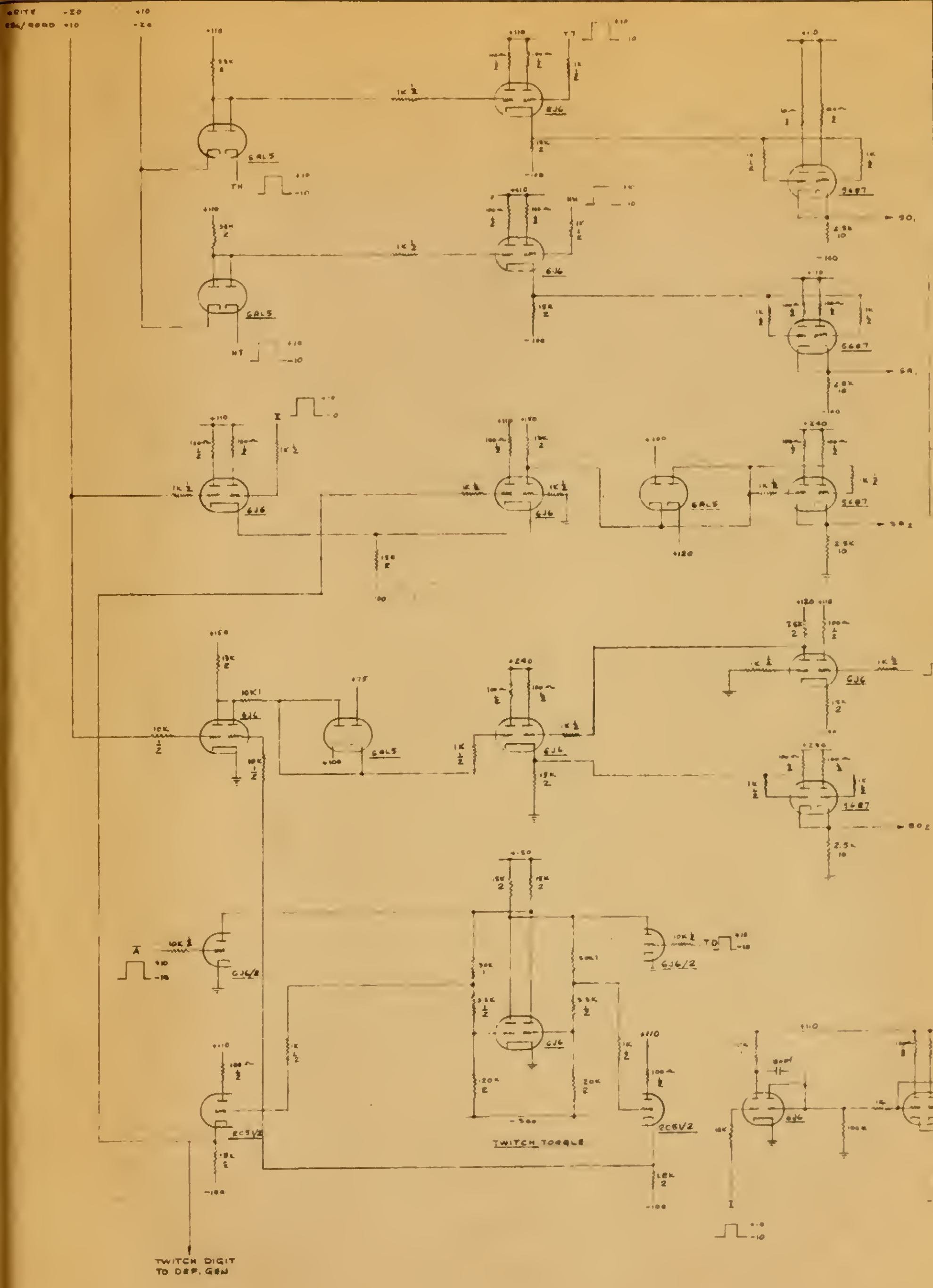
DIODE BUMPER STRIP SCHEMATIC
FOR 3 BIT RESOLVER OUTPUT

DRAWN. EMSLIE
DATE OCT 10, 1950
SCALE
DWG. No. 1238

D & W Blue Print Co



PER
DATE
2-8-51
3-11-51
CHANGE NO.

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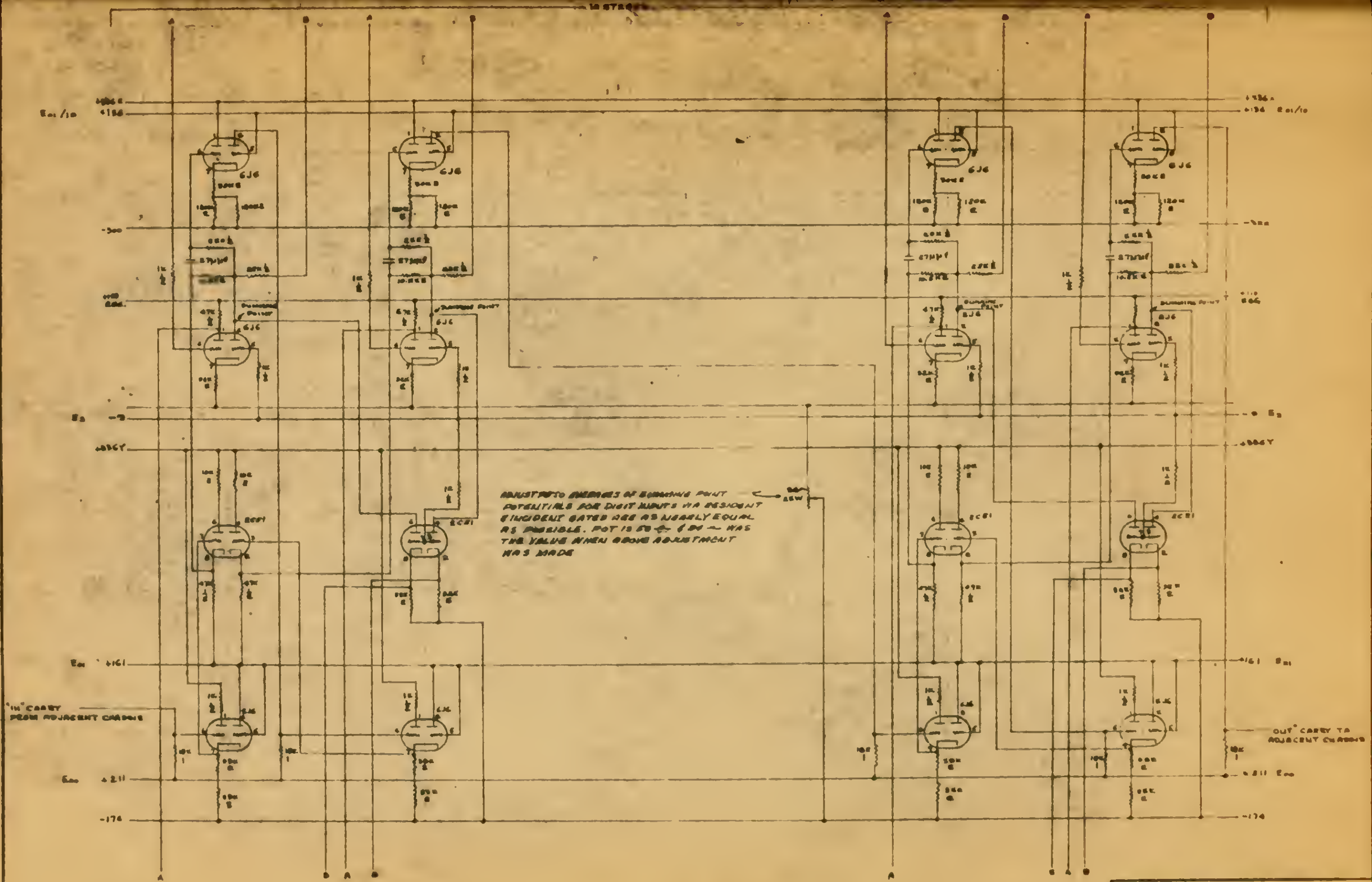
JP

DRAWN
DATE
SCALE
Dwg. No. 1325



ADJUST POT SO AVERAGES OF SUMMING POINT POTENTIALS FOR DIGIT INPUTS VIA RESIDENT & INCIDENT GATES ARE AS NEARLY EQUAL AS POSSIBLE. POT IS 50 K & 1 W ~ HAS THE VALUE WHEN ABOVE ADJUSTMENT WAS MADE

A - TO W. M. DISCRIMINATOR
B - IN ROOM COMPLEMENT GATES (INCIDENT DIGIT)

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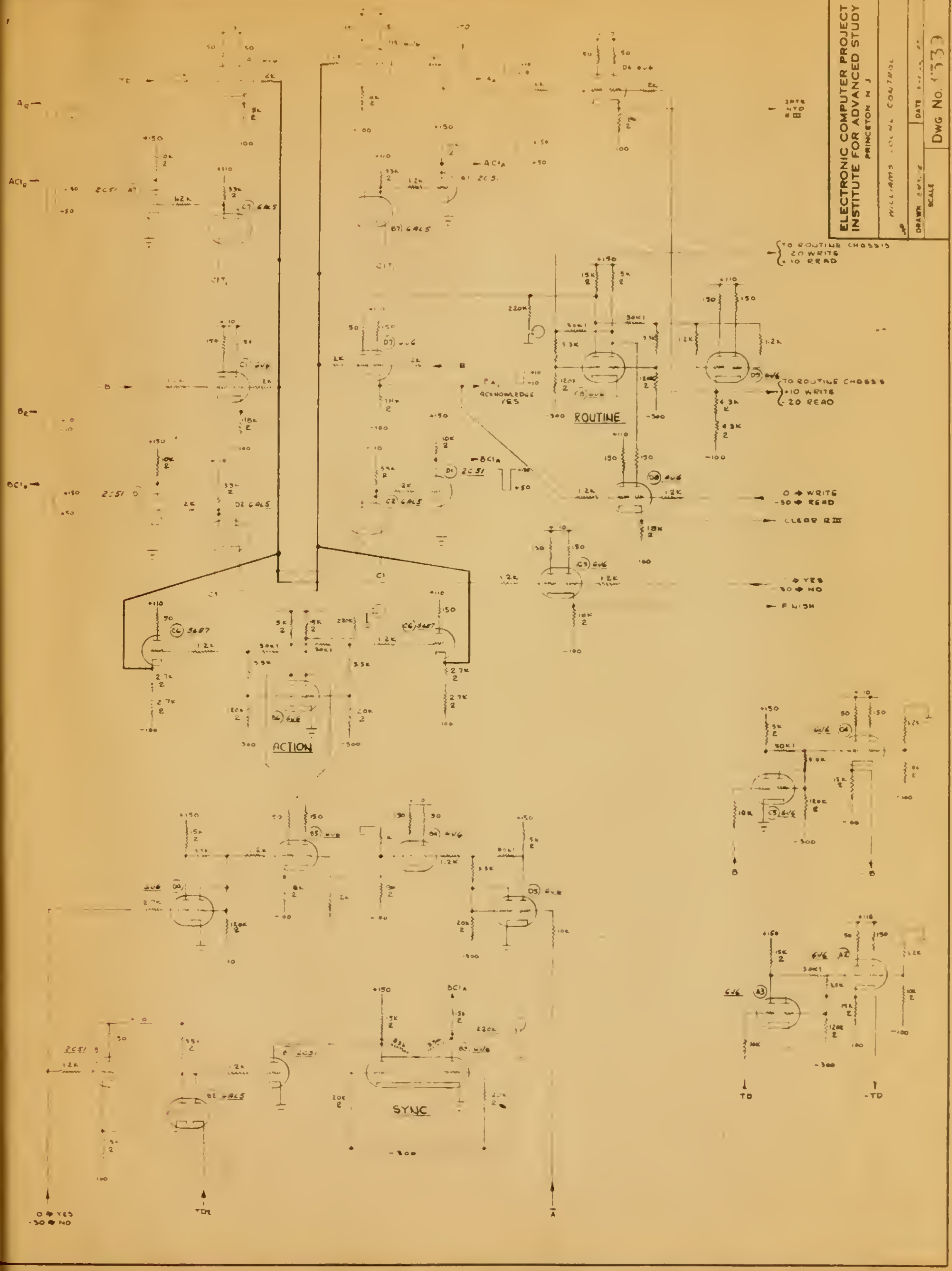
TYPICAL ADDER CIRCUIT
0 STAGES

DRAWN E MOLIG
DATE FEB 5, 1950
SCALE —
Dwg. No. 1334



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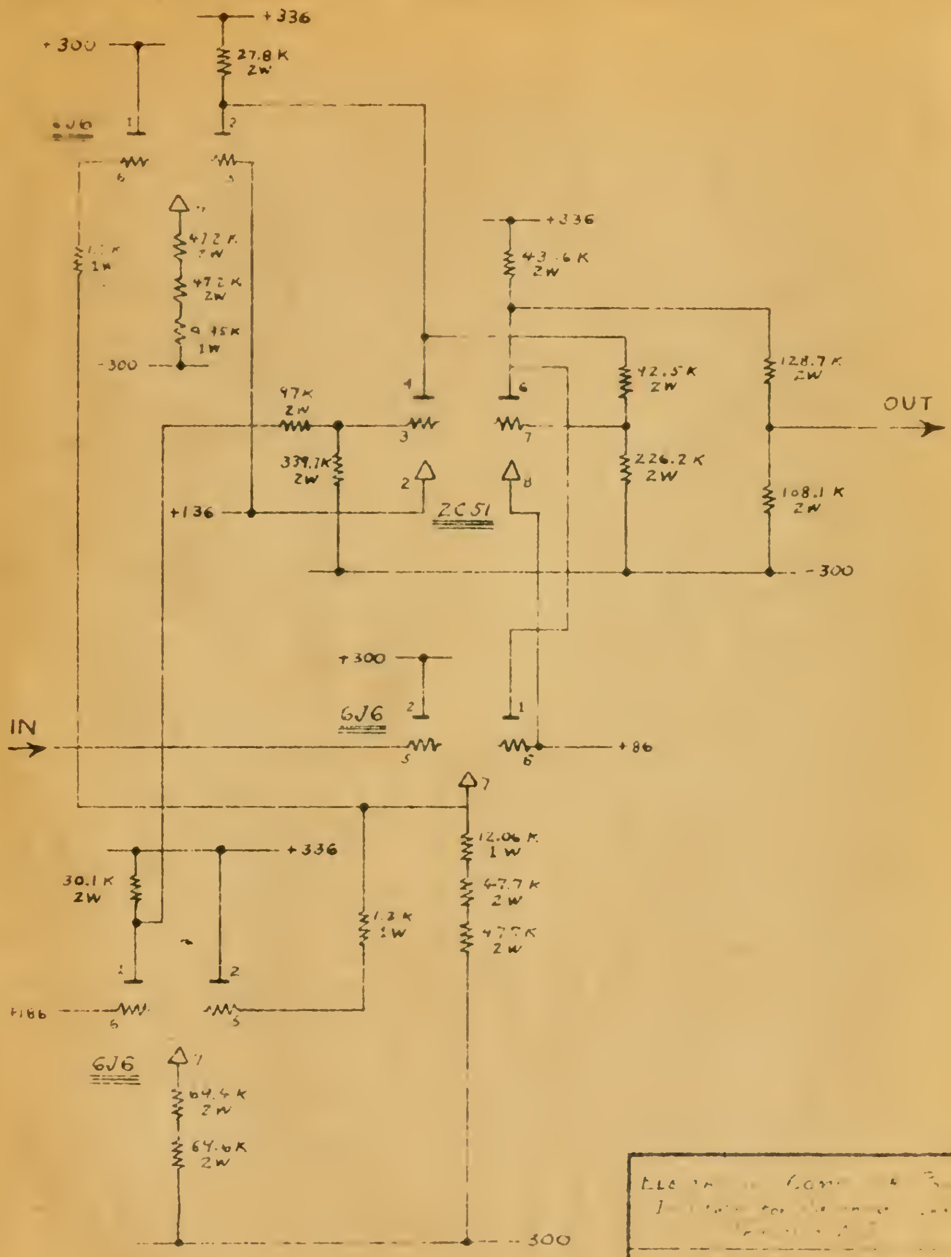
WILLIAMS COLUMN CONTROL

DRAWN
DATE
SCALE
Dwg No. 1733



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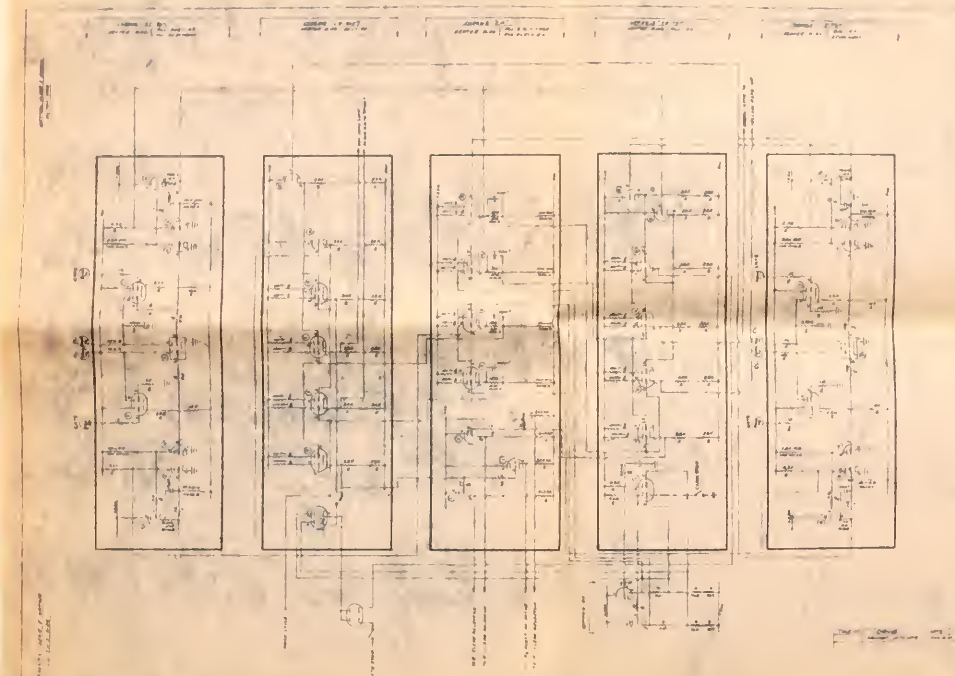
DIGIT RESOLVER
C-3-1107

[illegible] 28 [illegible]

[illegible]
H



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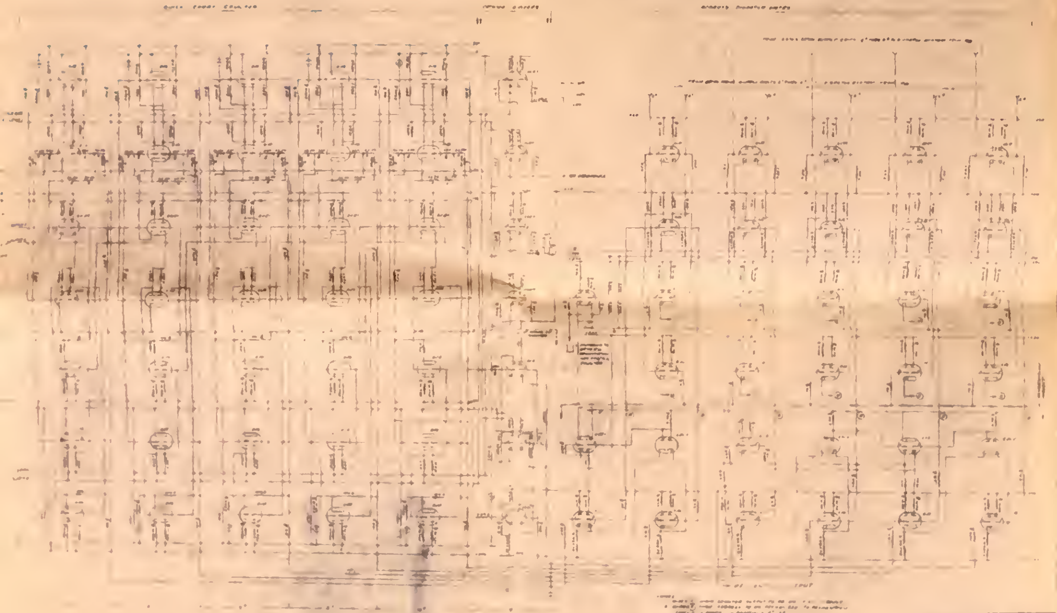
DWG No 1237



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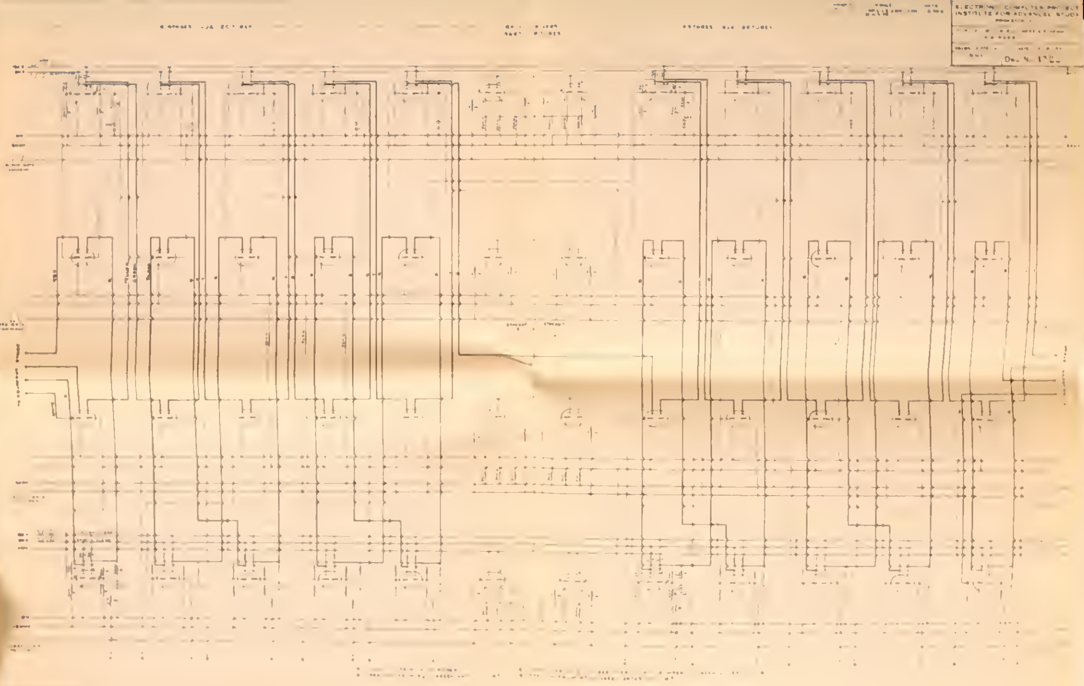
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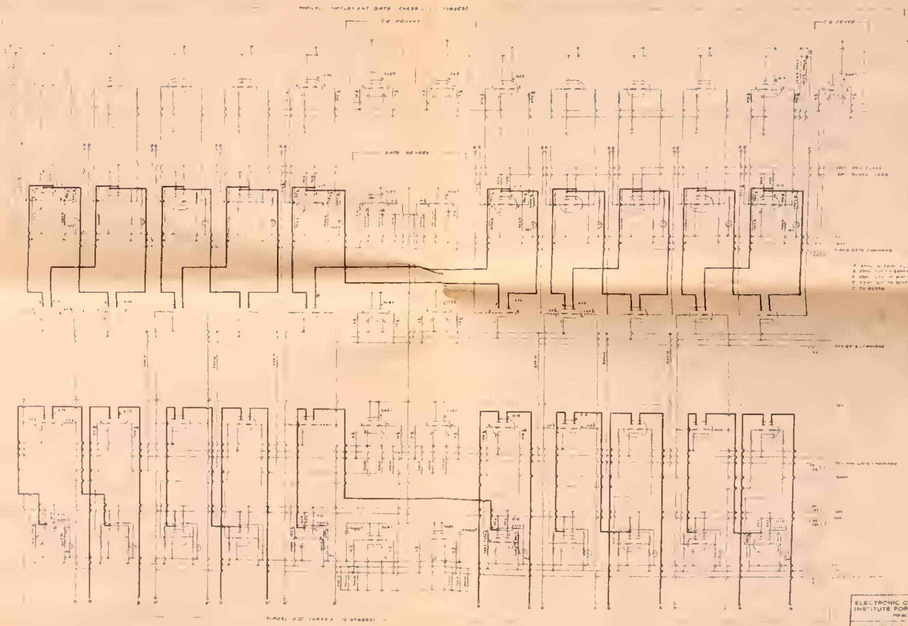

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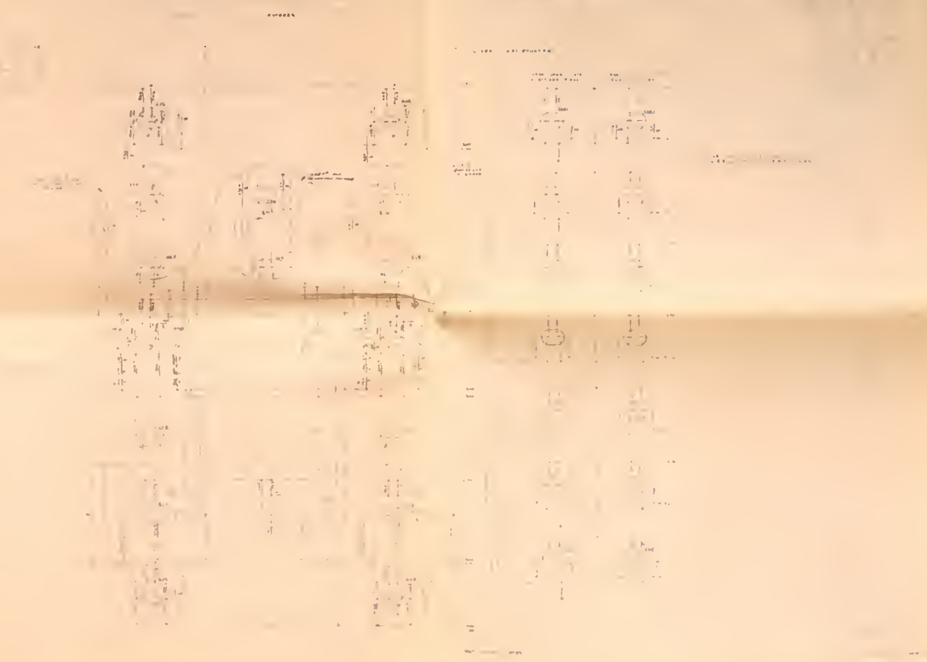
Dwg. No 1323



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Interim progress report.
v.6 [illegible]

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