SECOND
INTERIM PROGRESS REPORT
ON THE
PHYSICAL REALIZATION OF AN
ELECTRONIC COMPUTING INSTRUMENT

By

Julian H. Bigelow

Theodore M. Hildebrandt

James H. Pomerene

Richard L. Snyder

Ralph J. Slutz

Willis H. Ware

Institute for Advanced Study

1 July 1947

PREFACE

The ensuing interim report has been prepared in accordance with the terms of Contract W-36-034-CRD-7481 between Research and Development Service, Ordnance Department, U. S. Army and the Institute for Advanced Study. The express purpose of this report is to furnish contemporary advice to the Service regarding steps taken and contemplated toward the realization of an electronic computing instrument embodying the principles outlined in the following Institute for Advanced Study reports:

> 23 June 1946, by Burks Goldstine and von Neumann entitled, "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument." (Hereinafter referred to as L.D. 1).
>
> 1 April 1947, by Goldstine and von Neumann entitled, "Planning and Coding of Problems for an Electronic Computing Instrument". (Hereinafter referred to as P.C. 1).

The present report on the Physical Realization of the Computer is to be considered as a continuation of that listed above under the same title and employs the same nomenclatures and organizational plan.

The closing date of this installment -- 1 July 1947 -- finds the development group at the midpoint in several fundamental enterprises, and accordingly no attempt is made to present an integrated and comprehensive discussion of the entire problem of realization. Where specific progress has been made on various organs and components a brief account is given to convey the main facts; non-critical and transient detail being avoided whenever possible.

The experimental techniques, component types, schemes for synthesis of primary organs as well as the underlying philosophy of realization indicated in this report should be understood as wholly tentative, and are subject to revision from time to time either in detail or in their entirety as the work progresses.

J. H. B.

T. W. H.

J. H. P.

R. L. S.

R. J. S.

W. H. W.

TABLE OF CONTENTS

FIGURES

FIGURES (cont.)

DRAWINGS

TABLES

I. REMARKS ON ORGANIZATION

In January, 1947, the development group moved to its new quarters in the computer building, where many facilities became available. A small but adequate model machine-shop was set up, including a vertical and a horizontal milling machine, a surface grinder, small crank shaper, a medium and a small screw-cutting lathe, drill presses, welding bench, spotwelder, sheet metal brake and shear, etc. The shop model-making staff was increased to two when Mr. John Van Pelt joined our group; this arrangement has resulted in a very efficient and flexible unit, and is expected to continue. Two experienced wiring technicans, Mr. Lacey and Mr. Fell, constitute the electrical construction unit, and space is provided for several semi-skilled workers in anticipation of multiple assembly work of full-scale construction. The entire construction group of four is under the supervision of a production engineer, Mr. Richard Melville.

In February, 1947, two research engineers joined the group: Mr. Theodore Hildebrandt as a permanent addition, and Mr. Richard Snyder who remains with the group until September 1947. The engineering staff is consequently restored to the original quota of six, and was greatly strengthened by this addition.

The new building has provided adequate office space, conference room, drafting room, etc., and is considered to have been a great advantage.

II, GENERAL DISCUSSION OF COMPUTER

No essentially new ideas or changes of those presented in the earlier report have developed. It should be re-emphasized that the present limited objective of the development group is to produce at an early date what may be called a primitive model of the computer, having control features of less than optimum convenience. To this end several of the organs and components have been forwarded along lines of development less concise and more conventional than those indicated in section II of the report (P.R. 1) with a view toward advancing the date of primitive operation.

III. REMARKS ON THE REALIZATION OF LARGE MEMORY CAPACITY

No attempt has been made to advance in this direction since the January 1 report, except for certain tests and developments on magnetic wire recording, reported under section 5.

IV. MAGNETIC RIBBON EXPLORATION: TEST APPARATUS

4.1 LOOP SAMPLE COMPARATOR.

It may be recalled that this apparatus consists of a two-speed phonograph motor arranged to drive a loop specimen of magnetic recording wire (held in tension by a weight) over various recording heads. The speeds at which this apparatus was originally capable of operating ranged from one-half to several feet per second. However, experimental work in connection with the teletype input and output transcriber components (see Section VII) created a need for lower speeds; in particular, for speeds as low as one-tenth inch per second (two typed characters per second). Accordingly the apparatus was provided with a gear reduction to change

the time scale, and other mechanical improvements as indicated by Figure 1.

4.3 HIGH SPEED MECHANICAL DRIVE TESTER: FOR DEVELOPMENTS SEE SECTION VI: "OUTER MEMORY COMPONENT DESIGN STUDIES".

4.4 RECORDING-HEAD BOOSTER AMPLIFIER: FOR DEVELOPMENTS SEE SECTION VII: "INPUT-OUTPUT TRANSCRIBER COMPONENT STUDIES".

V. MAGNETIC RIBBON EXPLORATION: PERFORMANCE STUDIES

5.1 and 5.2 MAGNETIC PERFORMANCE AS FUNCTION OF SPEED.

As discussed in P.R. -1 under the above numbered sections, the primitive model computer must be able to record and reproduce pulse data on magnetic wire on both typewriter speeds (about 1 inch-second) and at "electronic speeds" (about 600 inches/second). However, in the primitive model computer it is planned to restrict the operation so that recording of typed (legible) characters onto the wire and their reproduction there from will be carried out only in uninterrupted runs from prepunched teletype tape (See section 7 to follow). Also, it is planned to load and unload the inner electronic memory (M_1) by means of the high speed wire drive outer memory (M_2) in uninterrupted runs at essentially constant speed (See Section 6 to follow). These two restrictions will result in a relatively clumsy mode of operation of the primitive computer, and will be wasteful of wire capacity as well as operating time. However, their disadvantages are considered temporarily tolerable in view of the many consequent simplifications and short-cuts in the apparatus.

Specifically, the continuous-run full speed exchange of data between M_1 and M_2 will permit the use of essentially simpler continuous speed single purpose mechanical drives in M_2 and also a simple low speed drive for

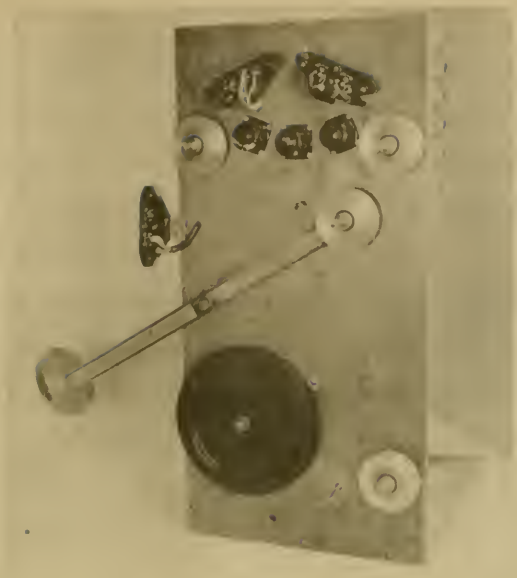


Figure 1
Low Speed Loop Sample Comparator, Mod 2

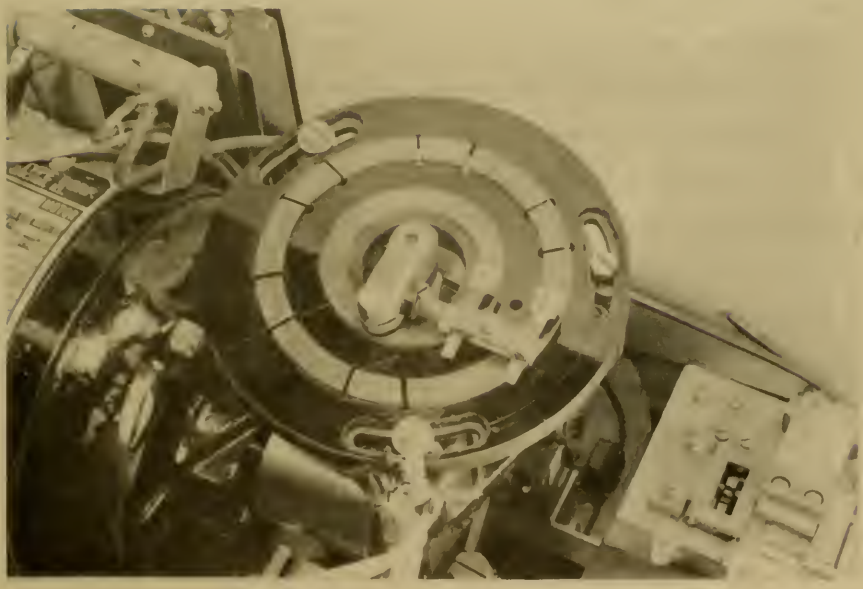


Figure 2
Special Transmitter Distributor

use with the teletype transcribing component. Furthermore, this restricted operation of the primitive model computer will permit construction of (essentially simple) single purpose electrical channels suitable only for the voltages produced at the two particular speeds selected. Other advantages accrue and will be discussed elsewhere.

However, this restricted mode of operation must eventually be obviated in any adequate model of the computing machine. The outer memory (M_2) must in the final model be automatically at the command of the control organ, being able to start, stop, reverse-and-hunt, etc., as the occasion demands. This will require complete speed flexibility of the drive system and electrical channels associated with M_2; and in particular the reversal requirement demands that the single electrical channel associated with M_2 must be able to handle with certainty wire voltage outputs corresponding to a speed range from 600 inches per second to as near zero as possible. This lower limit of speed (at which reading must still be possible) may be estimated by a crude calculation, based on the fact that at this minimum reading speed it must be possible to halt the rotation of the drive system within one-half word lengths on the wire; in order not to lose place. The closest packing now contemplated is two words (110 binary characters, including markers; see P.R.-1, section 7) per inch, so that the requirement is that the drive be halted within 1/4 inch, from minimum reading velocity. Using the relationship $g = V^2/2S$ it is trivial to calculate that if minimum reading velocity is one inch per second, about one-sixth gravity is needed to stop in a quarter inch, while if minimum reading velocity is ten inches per second, about sixteen times gravity is required. hence, if the electrical channel assoicated with the high speed drive system can operate reliably on voltage outputs corresponding

to two or three inches per second, the problem of preserving index through reversal of the wire drive presents no serious difficulty. Since reading at these low speeds is known to be feasible (see Section 5 of P.R.-1, also later sections of present report) no fundamental obstacle is to be anticipated when the automatic M_2 control is appended to the M_2 wire drive.

Some rough consideration should be given the problem of designing the electrical channel to be associated with the automatic M_2 in order to anticipate any difficulties that may arise. Conceivably, an electrical system could be designed which would operate on all electrical voltage outputs from the wire reading head, regardless of their amplitude, provided it exceed a certain predetermined minimum. Such a system would have in an early stage a purely binary cell, capable of producing at its output terminals a standardized "count" signal for any input pulse regardless of scale factor, provided only that it exceed threshold. In such a scheme, a fixed ratio amplification system could in principle be used for all reading speeds.

However, in considering such a scheme, the signal to noise ratio of the voltage output from the reading head must be taken into account. This ratio may remain nearly constant though both signal and noise voltage increase with speed, and in fact the noise level may be relatively higher at high speeds. Hence for a speed range of about 10^3 the noise at high speed may be expected to exceed the signal at low speed, so that a fixed voltage threshold binary counter would almost certainly be unsuitable. Accordingly, some means of introducing voltage gain correction in the amplifier channel (as a function of velocity)must be considered. This might be effected by a voltage takeoff tachometer on the wire drive system, arranged to introduce a linear term in the amplifier gain.

Accordingly, although the problem is not immediate, it was considered desirable to obtain a rough picture of how the peak voltage output of one or two representative magnetic wires would vary with speed, and whether normalization by a linear velocity term would produce a fairly constant scale factor. A few simple tests of this sort were carried out, using square wave inscription pulses, being careful to provide ample geometric spacing to keep overlap effects from being significant, and using frequencies thought to be well within the capabilities of the recording head. The results, normalized according to wire speed, are indicated in Table 1 below:

TABLE I

Wire Type	Speed in/sec.	Square wave cycles/inch	Output, average to peak uv/in/sec
BK 915	0.37	19.7	143
	0.865	19.7	171
	8.86	19.7	178
	20.8	19.7	171
NS 6828	0.37	19.7	47.5
	0.865	19.7	67
	8.86	19.7	74
	20.8	19.7	72.5
	600.	1.67	92.5

and appear to show that peak voltage output is roughly proportional to speed of the reproducing wire. The approximate constancy of the normalized voltage peak may be less valid for pulses of random sequence (instead of square waves) but the rough tests strongly suggest that an amplifier gain control containing a linear velocity correction would compensate for the greatest bulk of the variability in voltage level.

5.23 - 5.26 DEPENDENCE OF PACKING AND VOLTAGE OUTPUT ON DURATION AND AMPLITUDE OF RECORDING PULSE.

As remarked earlier, information in the form of a sequence of binary voltage pulses may be identified and signalled by means of a binary cell, responding alike to all pulses exceeding in amplitude a certain threshold. Any scheme of identifying non-periodic message pulses in the presence of background noise must rely solely upon the amplitude-time characteristic of the individual message pulse, which must differ distinctly from that of the background noise. Various means for distinguishing such pulses from background noise may be proposed, involving both linear and non-linear operations on the combined message and noise; and at some later date this point will be discussed more fully. In the meantime, it may be remarked that if the message pulse can be maintained high in amplitude relative to the background noise, during some specific interval of time, the problem of identification becomes greatly simplified; and in nearly all schemes of pulse recognition amplitude discrimination plays a dominant role.

Accordingly, peak voltage amplitude may be taken as a crude measure of pulse interpretability, and phenomena such as that of "pulse overlap" may be said to destroy interpretability in proportion as they affect peak voltage amplitude. More specifically, the proximity with which pulses may be packed

on a wire can only be discussed in terms of the penalty paid in the form of "loss of interpretability", which may be taken as proportional to certain particularly specified losses in pulse amplitude.

Consider the various forms into which the output voltage from the reading head may be cast (prior to interpretation), as indicated in Figure 3. If the voltage directly from the reading head is to be interpreted, the critical packing situation occurs when two pulses of opposite sign are adjacent; and the "Maximum safe packing" may be arbitrarily defined as that proximity at which the intervening discrimination valley has receded to one half peak pulse amplitude. Similar arbitrary amplitude thresholds of recognition may be set in the case of interpreting "differentiated" or "integrated" voltage waves, as indicated in Figure 3. An oscillogram showing actual overlap of voltage waves direct from the reading head, in the case of adjacent pulses of opposite sign, is shown in Figure 4A. These name pulses at a packing density corresponding to the arbitrary maximum of "one-half amplitude loss" in recognizability are indicated in Figure 4B. Oscillograms of differentiated and integrated pulses are given in Figure 5, A, B, C.

Having in this manner established arbitrary standards of pulse interpretability, it becomes possible to investigate the pulse packing density which may be placed on various samples of magnetic recording wire which will afford "standard interpretability",

The maximum packing at "standard interpretability" depends not only upon duration of the recording current pulse, but also upon

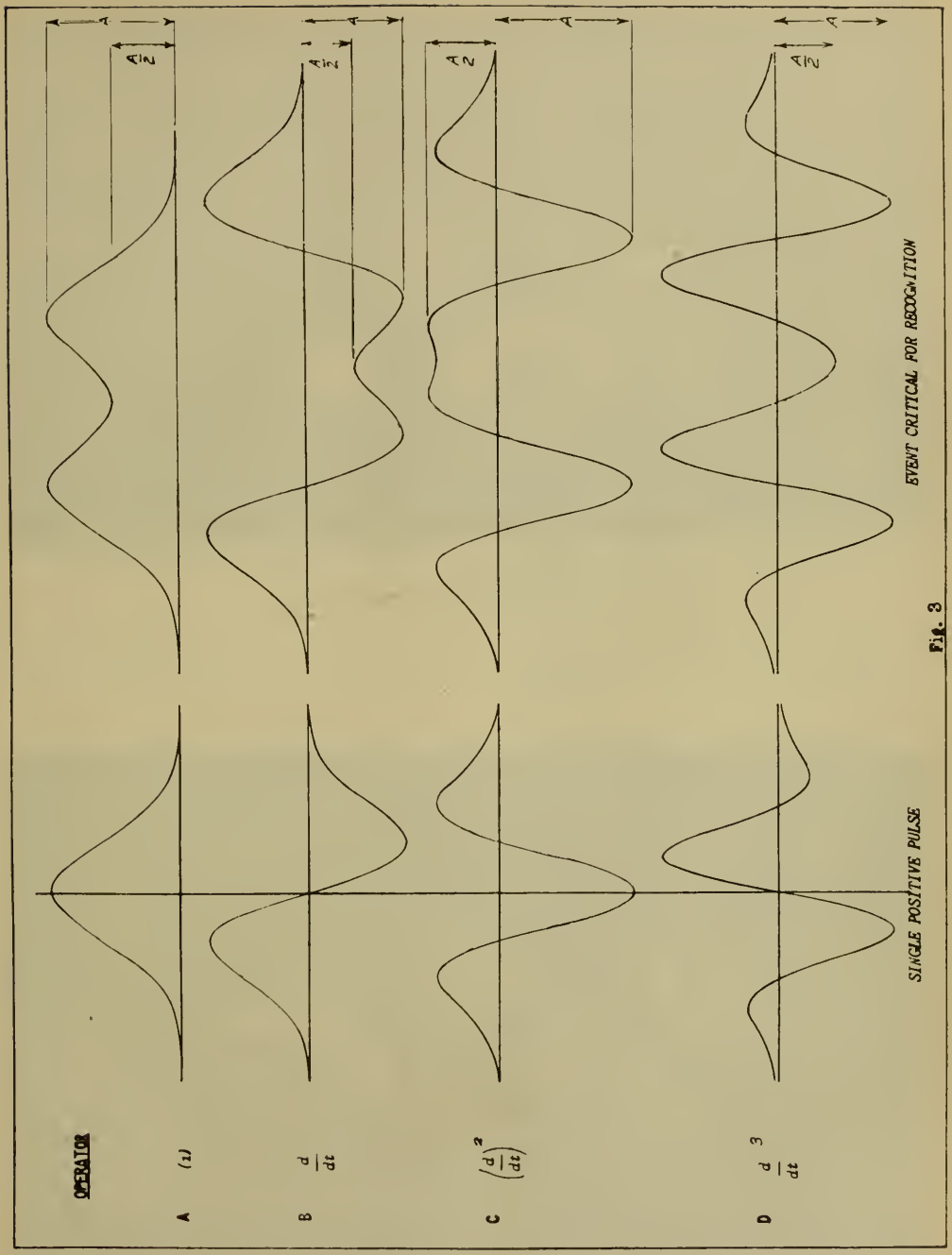


Figure 3
Recording Head Output Voltages

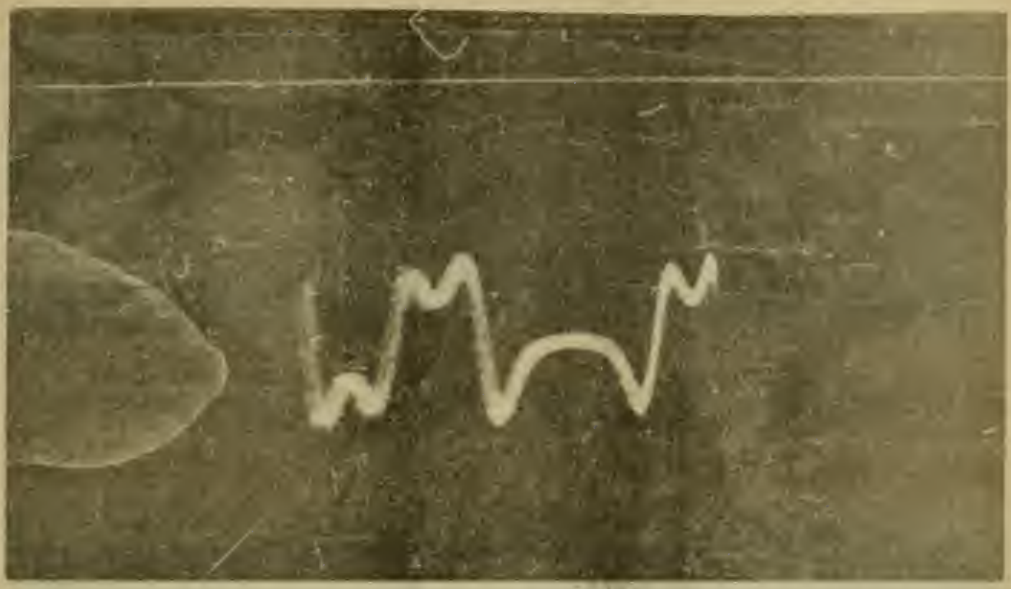


Figure 4A
Adjacent Voltage Pulses of Opposite Sign

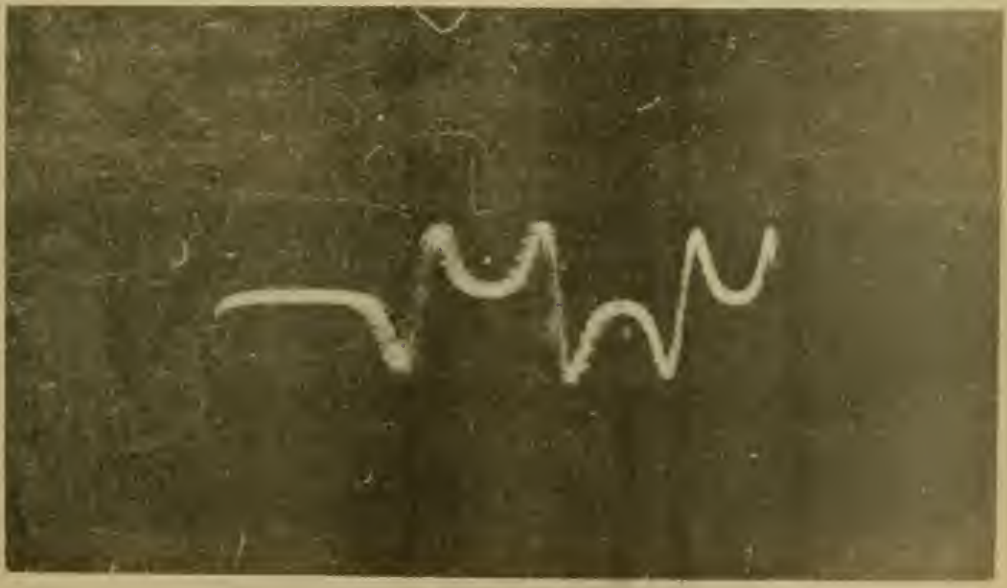


Figure 4B
Adjacent Voltage Pulses of Opposite Sign when

Output voltage direct from reading head. Three similar pulses spaced 141 to the inch. Recording pulse duration 8 microseconds, peak recording current 6.3 milliamperes.

Same pulses as above, restored by differentiation.

Same pulses as at top, restored by integration.

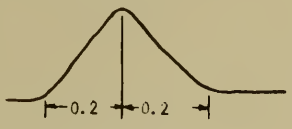
Figure 5 A, B, C.

Magnetic Wire Reproduced Wave Forms

recording current amplitude; and the reproduced voltage amplitude also depends upon these two factors. This relation was explored experimentally, using standard Brush heads and Brush BK No.913 wire. The apparatus used in this study consisted of the loop sample wire drive (4.1) and the recording driver (Section 7; also Diagram C-3-1009) which supplied current pulses of 8 to 800 microseconds duration to the head (waveform indicated in Figure 6B). For read-out purposes a pre-amplifier (Section 7; Diagram C-3-1010) was used in conjunction with a G.R. 714-A voltage amplifier; the output indicator being a Cathode Ray osoillograph.

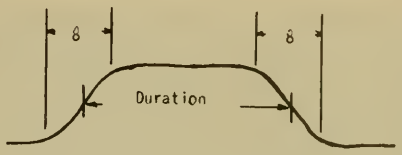
A plot of the observed relationship between "recording current" and "maximum packing" for standard interpretability is represented in Figure 7. This covers a range of pulse durations from 8 to 800 microseconds, and indicates a consistent increase (for all durations) in "maximum packing" as the recording current is reduced from about 12 to about 4 milliamperes. A "maximum" packing as high as 312 per inch results from pulses of 8 microsecond durations and 4 milliamperes recording current. It may also be seen that "maximum packing" increases constantly as pulse duration is reduced. (This family of curves, though as a whole consistent, is irregular in a few points, which may be attributed to error in observation of the C.R.O.).

In conjunction with the "Max packing" vs. "recording current" plots of Figure 7 it may be of interest to examine the "voltage output" vs. "recording current" relationship. This is represented by Figure 8, which indicates that while the head output voltage decreases rapidly with reduced recording current for pulses of short duration, the output voltage is relatively unaffected by recording current change for longer pulse durations.



Output of 1 MC. Pulse Generator
Driving 500 mmf. Load

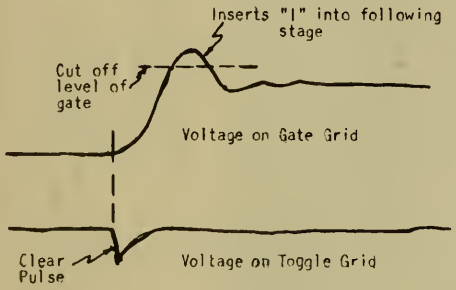
Figure A



All figures in microseconds

Waveforms of Current in Recording Head

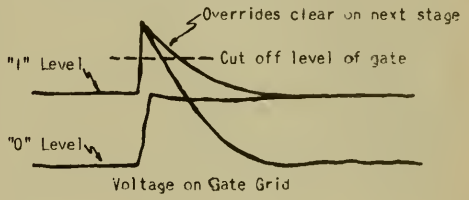
Figure B



Waveforms in Clear Type Register

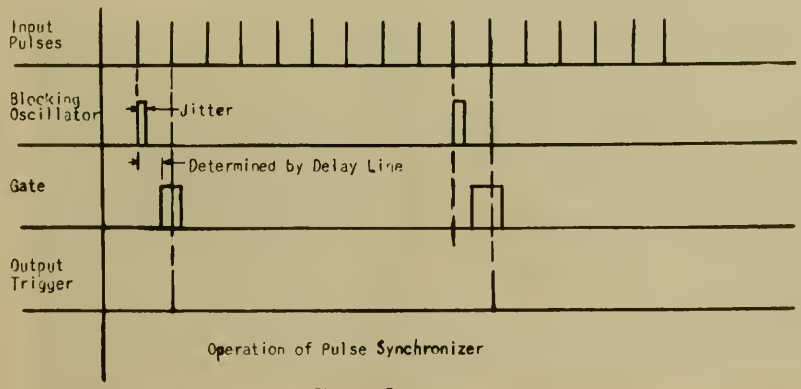
Figure C

Time constant of clearing pulse is equal to time constant of delay.



Operation of Conditiondal Clear Register

Figure D



Operation of Pulse Synchronizer

Figure E

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Figure 6
Register and Synchronizer Wave Forms

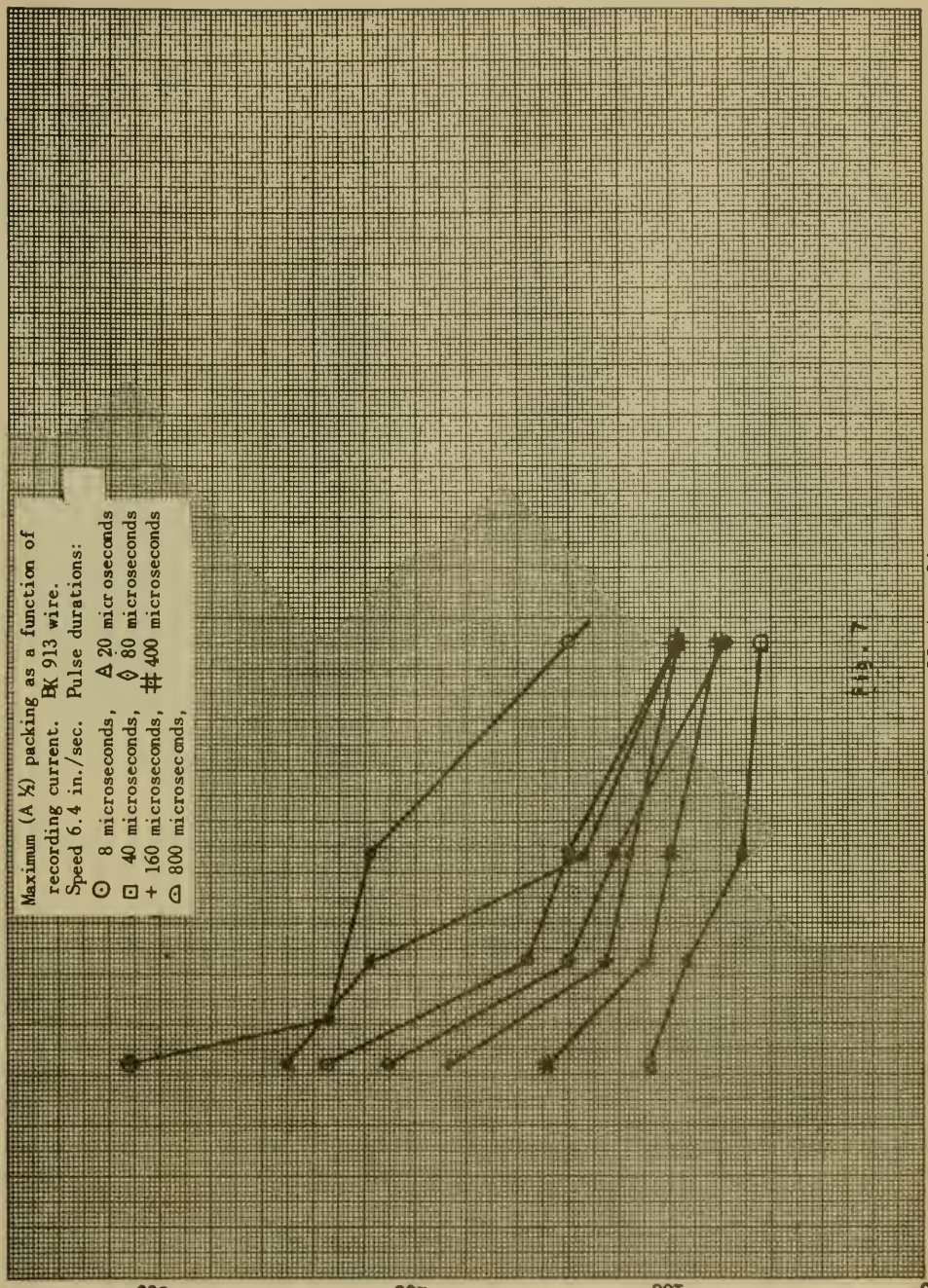

Maximum (A %) packing as a function of recording current. BK 913 wire.
Speed 6.4 in./sec. Pulse durations:
⊙ 8 microseconds, △ 20 microseconds
⊡ 40 microseconds, ◇ 80 microseconds
+ 160 microseconds, # 400 microseconds
◁ 800 microseconds,
Fig. 7
Maximum packing, pulses per inch
300
200
100
0
0
2
4
6
8
10
12
14
Peak recording current, milliamperes.

Figure 7

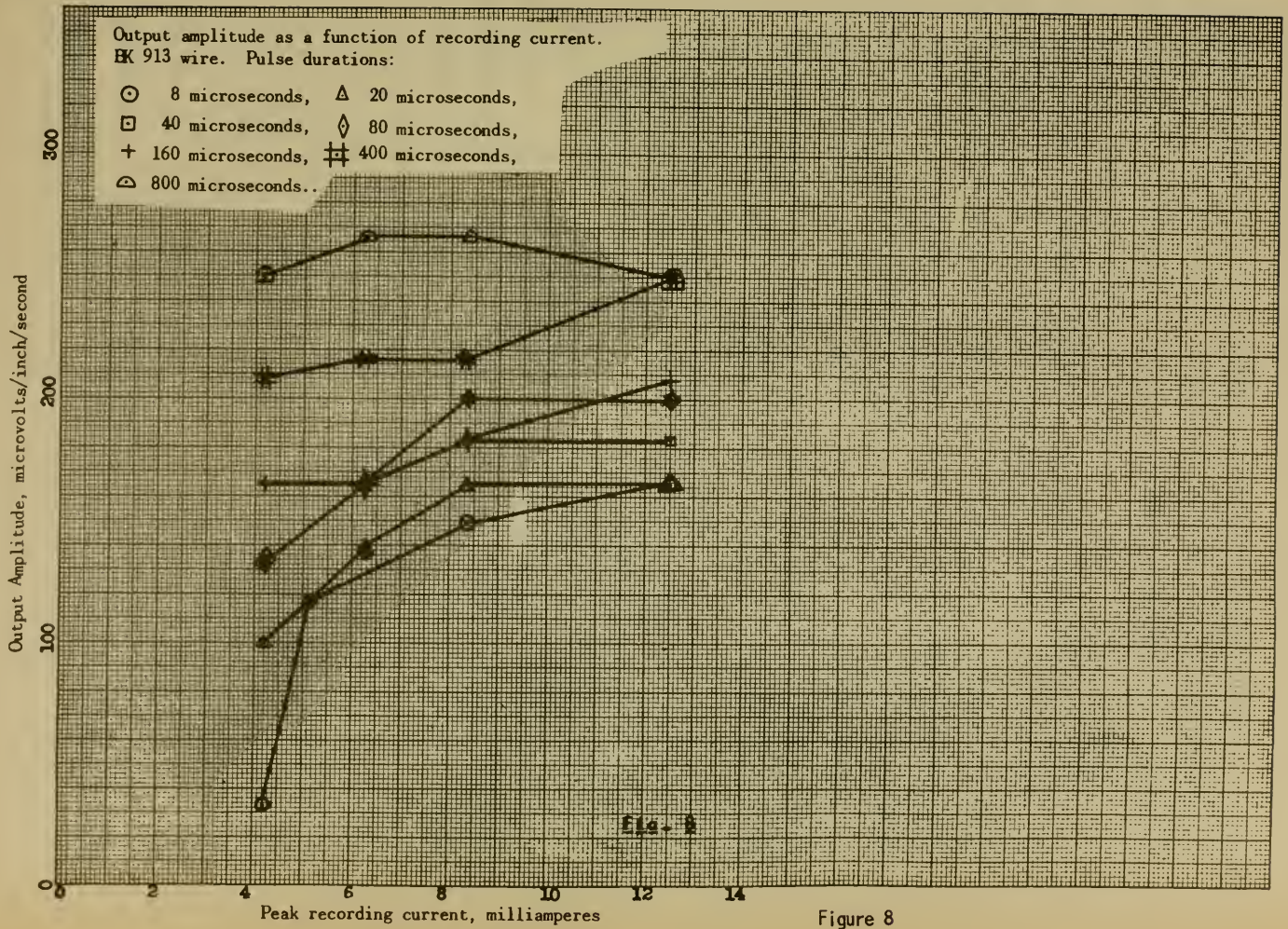

Output amplitude as a function of recording current.
BK 913 wire. Pulse durations:
8 microseconds,
20 microseconds,
40 microseconds,
80 microseconds,
160 microseconds,
400 microseconds,
800 microseconds..
Output Amplitude, microvolts/inch/second
0
100
200
300
0
2
4
6
8
10
12
14
Peak recording current, milliamperes

Figure 8

In fact, the recording current amplitude and duration conditions which produced lower "maximum packing" on Figure 7 appear to have produced voltage output pulses at the reading head which are relatively unaffected by changes in recording current from 4 to 12 milliamperes. Also, at lower recording currents, the maximum packing increases slightly but not abruptly. This suggests that it may be possible to explore experimentally the relationship between "maximum packing" and "voltage output" so as to find for each recording pulse amplitude and duration the highest output voltage at which the standard threshold of "maximum packing" is not violated. The results of this experimental attempt are presented in Figure 9 and seem to indicate that for BK 913 wire, all pulses having both relatively short durations (roughly 8 to 80 microseconds) and relatively low current amplitude (4 to 8 milliamperes) are roughly equivalent in their voltage output vs. packing density relationship.

Another relationship explored was that of peak voltage output at the reading head as a function of recording pulse duration; this is represented by Figure 10. It would appear that for Brush BK 913 wire moving 8.9 in/mc and excited by pulses of 7.5 milliamperes current, the peak voltage output at the reproducing head increases monotonically with duration of recording pulse, up to about 800 microseconds duration, and thereafter remains relatively constant.

5.28 COMPARATIVE PACKING OF WIRE SAMPLES

The most significant conclusion to be reached from the exploratory relationship presented in Figures 7-10 is that both the density of packing pulses and the voltage output of a given wire sample are related to each other and also to several other essential parameters; particularly, to recording pulse current and duration. Furthermore, it is clear that the system contemplated for pulse interpretation is a critical factor in judging the merits of any wire sample.

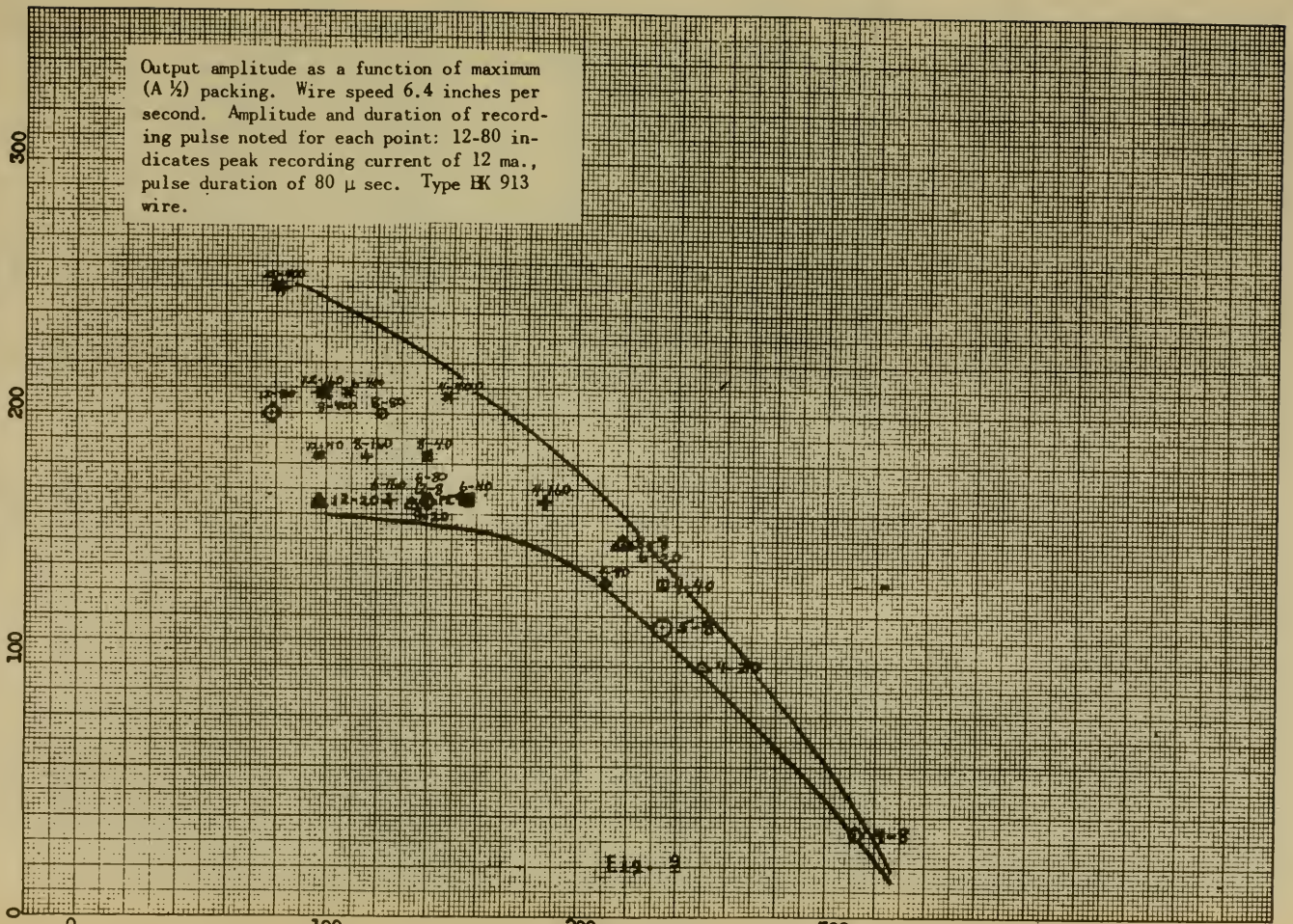

Output amplitude as a function of maximum (A ½) packing. Wire speed 6.4 inches per second. Amplitude and duration of recording pulse noted for each point: 12-80 indicates peak recording current of 12 ma., pulse duration of 80 μ sec. Type HK 913 wire.
Output Amplitude, microvolts/inch/second
0
100
200
300
A ½ Limit, Pulses/inch

Figure 9

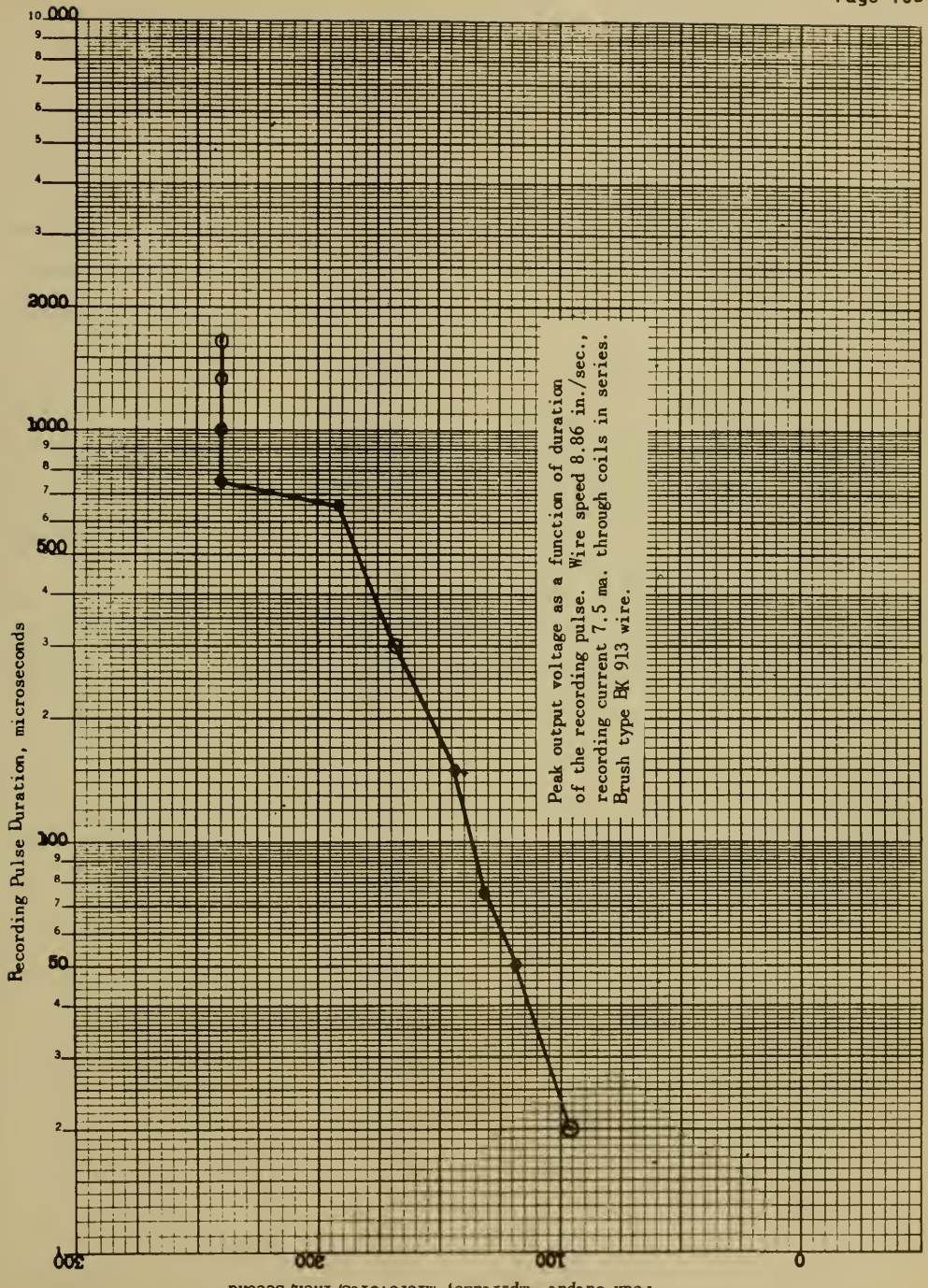

Recording Pulse Duration, microseconds
10,000
9
8
7
6
5
4
3
2000
1000
9
8
7
6
500
4
3
2
200
9
8
7
6
50
4
3
2
1
300
200
100
0
Peak Output Amplitude, microvolts/inch/second
Peak output voltage as a function of duration of the recording pulse. Wire speed 8.86 in./sec., recording current 7.5 ma. through coils in series. Brush type BK 913 wire.

Figure 10

Accordingly, a new comparison test was made between various samples of recording wire, the attempt being made in each case to find the "Optimum" recording pulse duration and current amplitude so as to maximize the voltage output without falling below the packing factor for standard recognizability; the methods used being experimental adjustment as in the case of Figure 10.

The results of this survey are given on Table II for 17 samples of wire, for schemes of interpretation of (a) the direct voltage output, (b) integrated voltage, and (c) the differentiated voltage output. In each case the relative output voltage is cited, together with the standard "maximum" packing.

It may be seen that the Brush BK 913 wire tentatively adopted as standard by the I.A.S. project, ranks high in both "maximum packing" (218 per inch) and voltage output (150 microvolts per inch per second)

TABLE II

Comparative Tests of Magnetic Wires

Wire Designation	Direct			Integrated			Differentiated		
	Recording Current (ma.)	Output uv/in/sec	A ½ lim. per inch	Output uv/in/sec	S 1/10 lim. per inch	S ½ lim. per inch	Recording Current	Output	Lim. per
G E Stainless A	29.2	67	83.4	6.7	82.6	139	29.2	5.8	187 S-½
Nat'l Stand No. 6630	18.3	116	133	3.3	86	156	5.0	5.0	390 S-3/4
G E Stainless C	14.2	50	136	4.16	93.6	156	8.3	4.2	312 S-½
Stainless 46	9.16	150	130	9.9	93.7	156	6.25	10	234 S-½
Cunico No. 331	16.6	215	172	11.7	125	218	7.1	11.7	390 S-½
Cunife 1 No. 327	23.7	300	148	16.5	109	188	12.1	20	390 S-3/4
BX 913 (Brush)	8.34	150	218	6.7	140	250	5.1	12.5	312 S-3/4
G E 315	20.0	116	156	6.7	106	187	8.3	8.3	250 S-½
G E Carbon Steel	12.5	183	48.5	29.8	43.8	62.5	5.0	4.2	83.4 S-3/4
Armour B614-6	15.0	150	48.5	26.6	40.6	59.3	4.2	4.2	109 S-3/4
Nat'l Stand A846-5	10.8	200	57.8	33.3	48.5	70.3	5.84	8.3	106 S-½
Brush BX906	8.3	123	78	16.6	73.4	109	5.0	5.0	218 S-½
Nat'l Stand Clarion No.6828	15	83.5	143	5.0	109	180	7.5	5.8	390 S-3/4
Toro (Swedish) 120-S	20.8	25	359	0.51	—	—	14.2	2.5	468 S-3/4
G E Stainless B	14.6	13.3	93.6	1.03	78	133	8.3	1.03	106 S-3/4
G E No. 176	22.9	150	108	13.5	90.5	140	7.07	8.34	344 S-½
Cunife D*		80	75	—	—	—	—	—	—

12.

VI. OUTER MEMORY COMPONENT (M_2) DESIGN STUDIES

It was proposed (in the corresponding section of P.R. -1) that the High-Speed Wire Drive apparatus be modified so as to meet the requirements of the outer memory component M_2. The basic principle of direct shaft drive to both loading and unloading reels was to be preserved, together with the scheme for differential-servo slack takeup operating from a low inertia constant-tension loop follower. The main changes contemplated were:

(1) To use particularly designed reels of smaller diameter (6 to 10 inches);

(2) To provide a wire capacity of about 10 cubic inches;

(3) To improve the servo design to extend the operating range up to speeds as high as possible;

(4) To provide certain automatic features such as level winding, automatic parking brake, head engagement and adjustment, etc.;

(5) To engineer the device with sufficient care and skill so that it would give trouble-free service under continual usuage.

The first step in this development program was to design a true-scale plate model, having all essential parts in true dimension, but fabricated insofar as possible from standard catalogue parts and standard shapes, etc., avoiding the use of special castings, special motors and the cutting of special gears. Such a plate model was designed, constructed and tested in our model shop, and is pictured in Figures 11A and B. Three castings only were used: (1) the reels, of dural; and (2) the experimental servo-motor mount, of dural; and (3) the level-winding traverse beam, of magnesium alloy.

Although in the first "production"model of this component it is planned to use a servo-motor of the polyphase induction type, having double shaft takeoff to drive both reels, the plate model was built with two Delco internally-geared direct current permanent magnet motors, operating

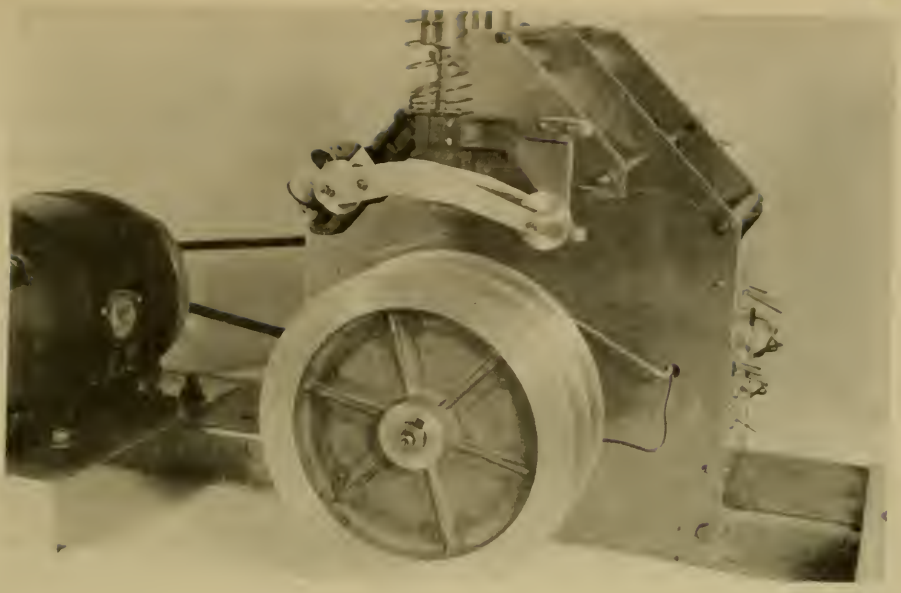


Figure 11A
Plate Model, M2 Wire Drive showing Level Winder

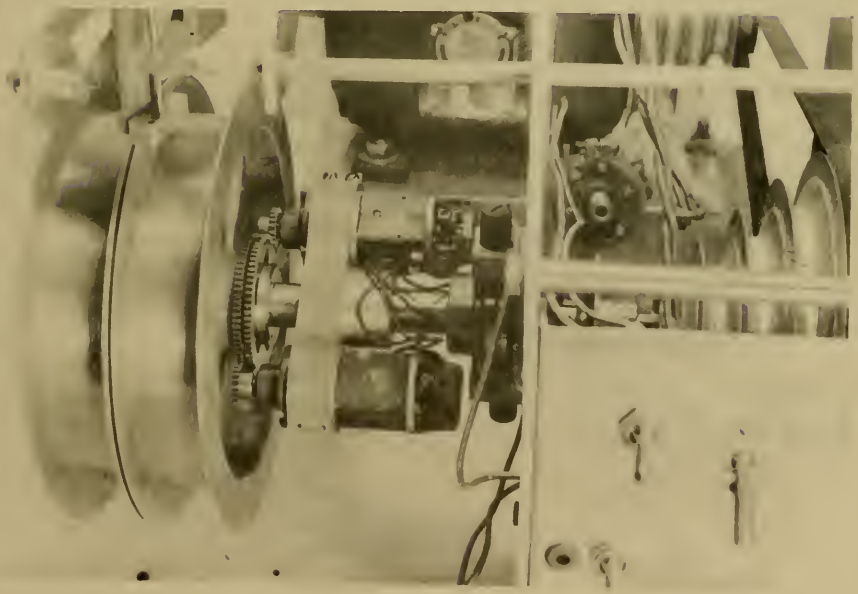


Figure 11B
Plate Model, M2 Wire Drive showing Experimental Differential

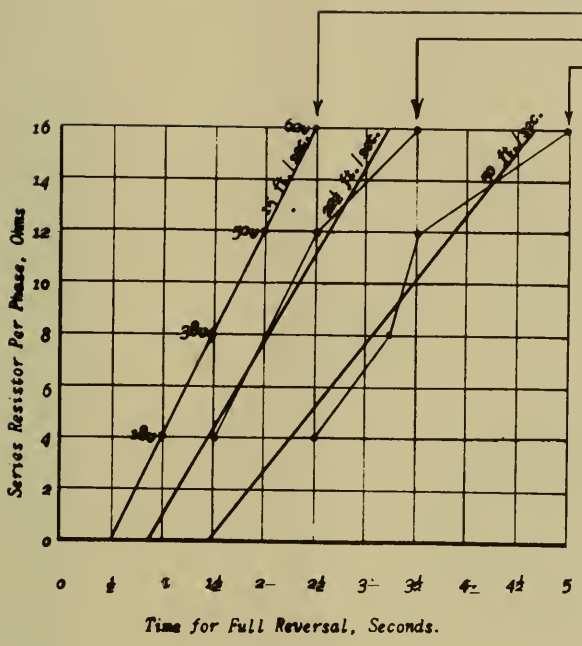
a differential composed entirely of standard "Boston" gears; this arrangement being thought more flexible in speed of response, and hence more suitable for experimentation.

The differential arrangement used in this plate model (and planned for the "production" model) controls the loop size by driving the two reels in opposite directions, so that slack is paid out or drawn up by opposite motion of the reels relative to the main drive shaft. As a result, the activity of the differential motor system does not react on the main drive shaft and motor, except for small higher order effects, such as that due to the difference in moment of inertia of the two reels when one is loaded with wire and the other nearly empty. This difference in moment of inertia is small compared to the total, and the force of reaction it produces is relatively even smaller because of the small acceleration of the slack-takeup. Additional advantages of this servo system are that the ratio of loop control to acceleration is minimized; that it is symmetrical with reference to direction of wire feed, etc.

As a whole, the plate model operated quite well at speeds up to the prescribed 50 feet per second wire travel. It was operated at about this speed with full wire capacity for several hours in the model shop; the particular wire used being far more frangible than the BK913 currently considered the most likely candidate for adoption as standard. The traversing scheme for level winding proved quite satisfactory; it is not intended to wind in layers but produces a dense random wind of uniform height for all speeds and directions. It is considered that the principle of pivoted traverse system is well suited for the final model.

The constant-tension slack follow-up system tried in the plate model made use of a sliding arrangement whereby the entire traverse beam shifted vertically with spring tension to follow up the loop motion. This system operated fairly well but was not completely satisfactory, inasmuch as it had a tendency to vibrate and "hop" at certain speeds, due partly to unfavorable mass vs. elastance ratios, and partly to the familiar "stiction" of sliding motions, plus some contribution from the relatively flimsy mechanical construction of the plate model. As an alternative, a pivoted-motion follow-up similar to the prototype model was tried, and found more satisfactory, and is expected to be used in the final model. (See Figure 13, assembly drawing, tentative M_2 component, Mod. 1).

Tests were carried out on this plate model to determine approximate acceleration and reversal performance. In the first of these tests, the one-half hp 3 phase drive motor was full-reversed by phase transposition at full speed; this high acceleration together with the impulse load resulting from some play in the differential system was too much for the interval gearing of the Delco motors, and stripped the teeth. This was of course of no consequence inasmuch as that part of the model is structurally an experimental substitute for the final design. The motors were replaced, the backlash removed, and a new sequence of reversal tests started, this time placing a series resistor in each phase of the maindrive motor. The resulting "Elapsed times for complete reversal" are indicated in Table 3, and include readings at full reversal acceleration (without series resistor) made possible by eliminating backlash.



REVERSAL PERFORMANCE
OF
WIRE DRIVE

Table 3

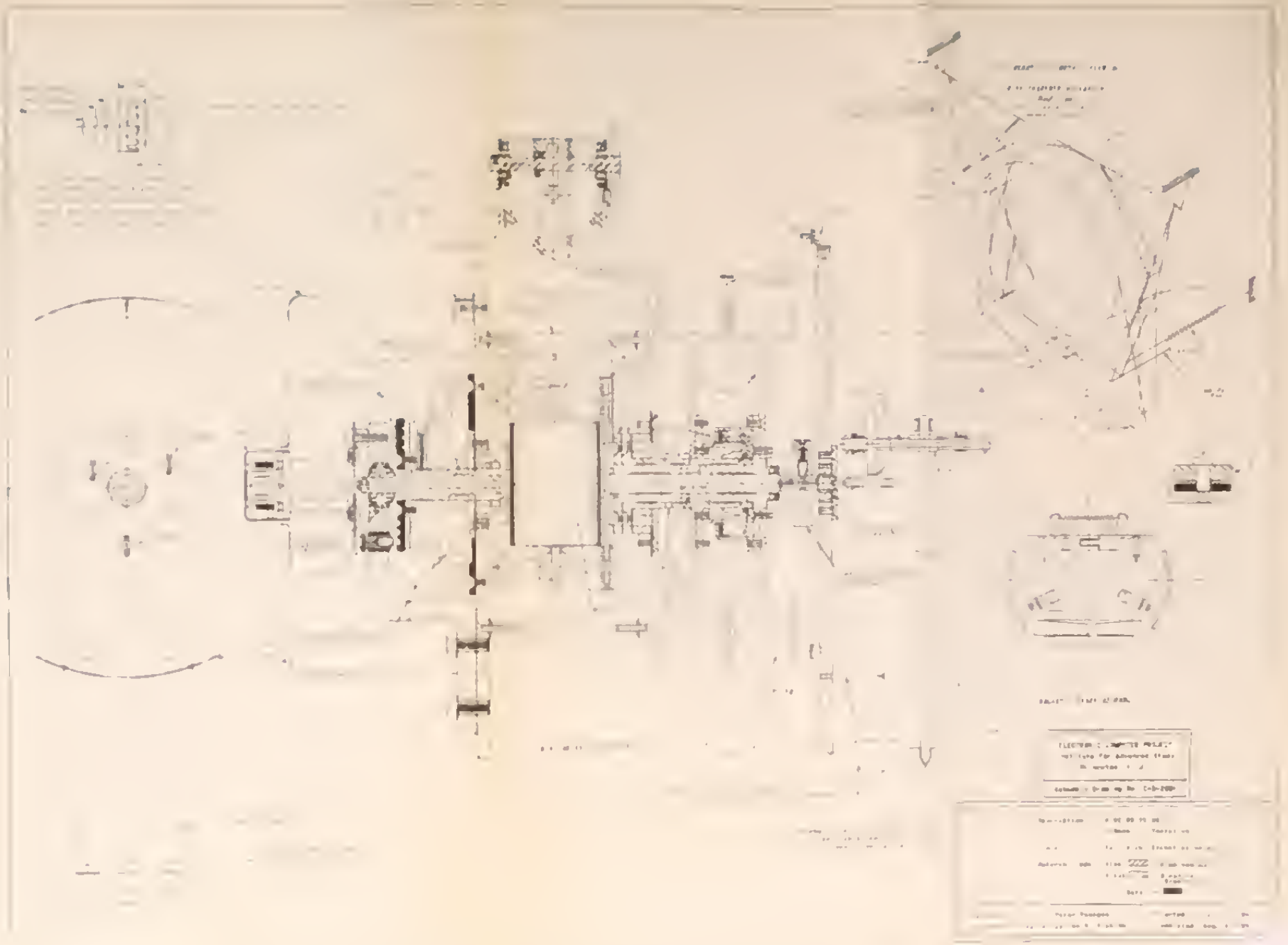


Figure 13

As indicated, the drive motor without series resistor is capable of reversing the entire system from 50 ft/sec in one direction to 50 ft/sec in the other direction in roughly one and a half seconds. Very roughly, two-thirds of this reversal lag may be attributed to the inertia of the reel drive system, and one-third to the motor and drive pulleys. It is expected that the "mod. 1" design of Figure 13 will have less than half the moment of inertia of the plate model, and will be structurally strong enough to give reversal times of less than a second. However, taking the attained reversal rate of one and a half seconds as the value realized, it would appear that the penalty in reading rate due to a reversal would be to attain an average reading velocity of roughly 25 feet per second for one and a half seconds, equivalent to a loss of 3/4 second at full reading rate.

The "tentative Model 1" design of the M_2 component has been carried essentially to completion (see Figure 13, Assembly layout) and construction of the first unit is about to begin. As may be seen, this component has provision for unit assemblies of the main drive motor, main differential drive, reel assembly, follow-up and traverse system, and magnetic wire compartment. It is anticipated that this arrangement will facilitate any later modifications not presently planned. A chart of the servo-motor performance in terms of the main drive speed is given in Figure 14, and indicated performance to be anticipated at speeds beyond the present goal of 50 ft/sec.

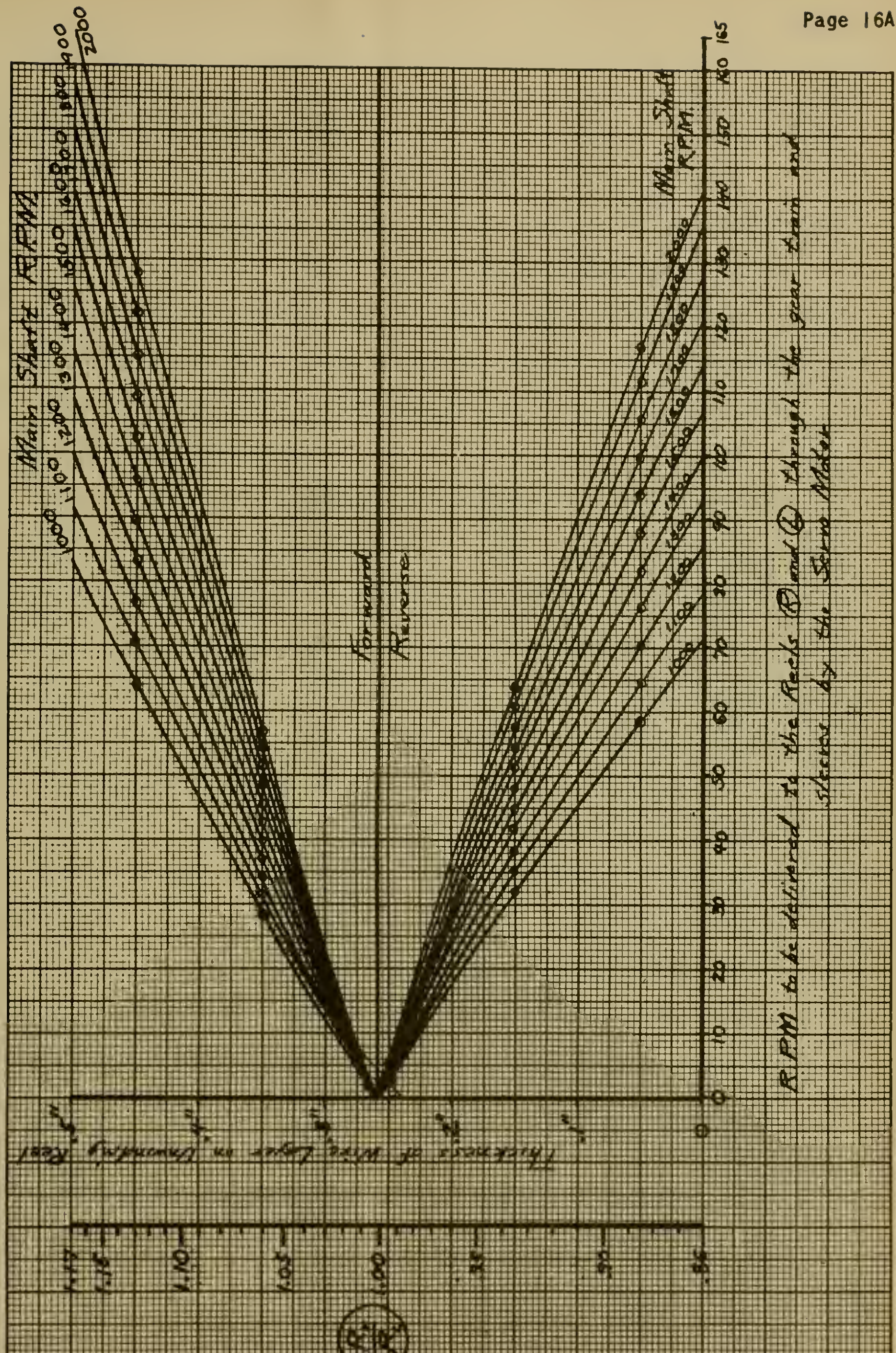

Main Shaft RPM
Forward
Reverse
Thickness of Wire Layer on Unwinding Reel
Main Shaft RPM
RPM to be delivered to the Reels (R) and (L) through the gear train and sectors by the Servo Motor

Fig. 14

VII. INPUT-OUTPUT TRANSCRIBER SYSTEM

As discussed in the corresponding section of P.R. 1, a rather highly efficient input transcriber system, from both the logical and instrumental viewpoint, would consist of two or more keyboard stations (or a single station used repetitively) at which data and coded orders would be transcribed directly onto the magnetic wire. With such an arrangement, the transcription operation could be checked and corrected immediately upon the magnetic wire before releasing for "publication".

Such a system would necessitate development of a special keyboard transcribing unit, involving the equivalent of a moving magnetic head arranged for immediate playback, verification and correction. While it is planned eventually to develop such a system, it was considered expedient to devise a somewhat less efficient system which could be made operable at an early data. A substitute system of this sort based on modification of standard teletype components is indicated in Figure 15.

The system represented by Figure 15 utilizes teletype punched tape as an intermediary between the essential keyboard and essential wire recording operations.

The logically and instrumentally redundant tape operation is introduced primarily to facilitate verification of the (human) keyboard operation against itself, and to permit correction of errors thus found; it being thought that this step is more subject to errors than are mechanized processes. By introducing this redundant tape storage medium, new classes of possible errors are introduced, such as in reading into and out from the tape; furthermore the tape is far less convenient medium upon which to verify and correct errors

than is magnetized wire. Finally, the problem of verifying the transcription onto wire is in no way facilitated by the introduction of perforated tape; it is merely deferred until it can be handled by an over-all feed-back operation of the wire through a print-out system; at which stage correction of the wire is not at all convenient.

In full cognizance of these merits and demerits, it has been considered expedient to push the development of an input-output system such as that represented by Figure 15, and this program is, in fact, nearing completion.

Referring to Figure 15, the upper chain represents the "Input" process, and is divided into two physically and temporally independent sequences: (1) The relatively slow operation of manual transcription (with proof-checking) from manuscript to keyboard to punched tape to wire (M-2). (2) This is followed by the more rapid operation (1000 words/sec.) from magnetic wire (M-2) to shifting register to selectron memory (M-1). The corresponding "Output" sequence consists (1) of unloading the selectron memory (M-1) at high speed onto the magnetic wire (M-2), and then transcribing at low speed from magnetic wire to perforated tape to printed manuscript.

Both slow (printing or keyboard speed) operations can be carried out at sites with equipment independent of the computing machine proper. This is of practical importance since these two operations, being essentially slow and likely to remain an irremovable bottleneck, can be made faster only by parallel duplication of setup; and this should not encumber the proper function of the computing machine. It is planned that during these two slow operations, the wire drive speed will be so low (circa 1/4"/sec) that continuity of operation is not necessary, it being possible to start and stop without loss of

information (in the case of printing) and to tolerate wire wastage resulting from continuous feed during brief interruptions in the case of recording. Accurate wire speed control during either slow process is of no advantage, it being necessary merely to accelerate from zero to minimum reading velocity within short enough distance to avoid loosing information.

Equipment to carry out the two slow operations (Steps 0-6 and 18-25 in Figure 15) is being developed for the Institute for Advanced Study project (and for others) by the Bureau of Standards computer group. Specifically, it is expected that they will furnish a pair of modified teletype keyboard transcribers (1 and 2) each producing a perforated tape; and for the comparison of these will provide a special teletype tape comparator (3) which will generate a third, or "proofed" tape in the event of agreement between 1 and 2, and which will provide for automatic interlock in the case of disagreement, affording means for manual error diagnosis and correction, interlock release and subsequent issue of "proofed" tape. The Bureau will also furnish a transmitter-distributor (4), recording head driver amplifier (5) and low speed magnetic wire transport with recording head (6). For the"printing out" sequence, a low speed wire transport (18) will be provided, together with reading head and suitable voltage amplifiers (19) pulse shapers and interpreters (20-23) commutating tape punch (24) and printer (25).

This equipment is expected to be available from the Bureau in the near future. Meanwhile the group at IAS have nearly completed the apparatus involved in the two high speed sequences (7-14 and 14-17) and also have devised makeshift equipment for interim use capable of carrying out the two low-speed operations. This equipment will be used for various preliminary tests

in anticipation of apparatus to be furnished by the Bureau. A brief account of these developments will perhaps be most effective if reference is made to Figure 15, describing what has been accomplished at each step.

Referring to Figure 15, steps 0 through 3 produce teletype tape punched with data and orders in five-bit binary code. A single teletype transmitter is capable of carrying out this over-all function, with practically no modification, provided visual checking of typed or perforated characters be effected. We have set up a teletype transmitter and arranged it to carry out this function.

Step 4 consists of a teletype transmitter distributor arranged to read the punched tape, and to issue corresponding time-sequence pulses suitable for recording on magnetic wire. The standard teletype transmitter-distributor carries out exactly this function in the desired five-bit code, except that the standard time sequence does not provide merely five regular code pulses, but also a "commence" and "conclude" pulse. To delete these so that they will not reach the magnetic wire, and to spread the five code-pulses evenly in time requires merely the replacement of the standard distributor commutator by one having five regular segments, and this was accomplished as indicated by Figure 2.

Having thus provided means to convert the information to electrical form in proper time-sequence, the next operation is to recast it into uniform, brief pulses of high amplitude, suitable for recording on the magnetic wire. Since the repetition rate of these pulses is quite low, this operation was easily realized by means of a balanced thyratron circuit, involving two miniature 6D4 tubes electrically symmetrical with respect to zero voltage level, each filtered on the input and driving with its output a separate half of the

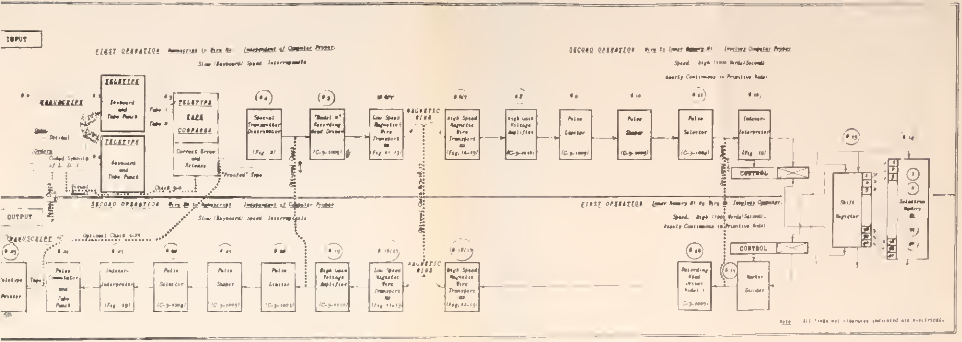

INPUT
OUTPUT
FIRST OPERATION
SECOND OPERATION
TELETYPE
MANUSCRIPT
MAGNETIC WIRE
CONTROL
CONTROL

Figure 16

recording head winding. (See diagram C-3-1009.) This device constitutes step 5 in Figure 15 and is called "recording-head driver, Mod. 2". (In fact, so effective is the Mod. 2 driver amplifier in producing brief pulses of high amplitude from pulse data of low repetition rate, that output cannot be viewed by the usual neon indicator tubes because of insufficient pulse duration. Accordingly an auxiliary device, called a "pulse viewer", has been developed (Figure 21, drawing C-2-1014) to prolong these pulses and permit them to be seen on neon indicators.)

The next operation required in step 6 of Figure 15; here the pulses are applied to the magnetic recording head, held in contact with the slow-moving magnetic recording wire. This operation may be carried out on the low-speed loop-sample comparator (Figure 1) in case of tests involving brief messages, or on the high speed wire drive plate model (Figure 11 B shows the small auxiliary worm-drive motor at end view) and furthermore means will be provided for this function on the final model of high speed wire drive (Figure 13). It may be noted in passing that since the transmitter-distributor (4) infers from tape and issues electrical pulses at a fairly regular rate, the velocity of the low speed wire transport need be only roughly constant.

The next operation initiates the high speed (1000 words/sec) sequence, starting with the high speed wire drive (M-2) of which the prototype (see P.R.1) and plate model version discussed earlier in this report (Figure 11) are now operable, and the "production" model (Figure 13) is under construction. From this step (6/7) the information issues in electrical form to step 8, the high-gain preamplifier (Figure 16) which may be seen from diagram C-3-1010 to consist merely of a transformer input triode voltage amplifier stage which drives the

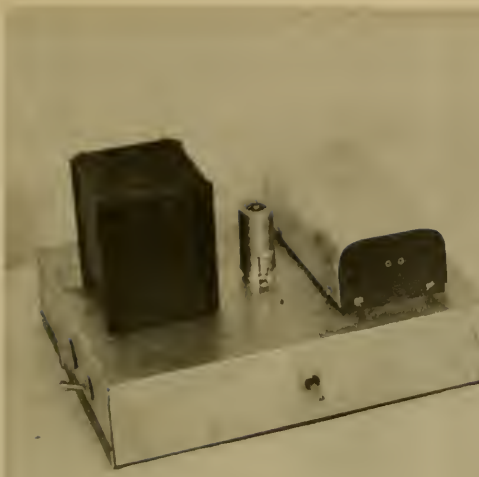
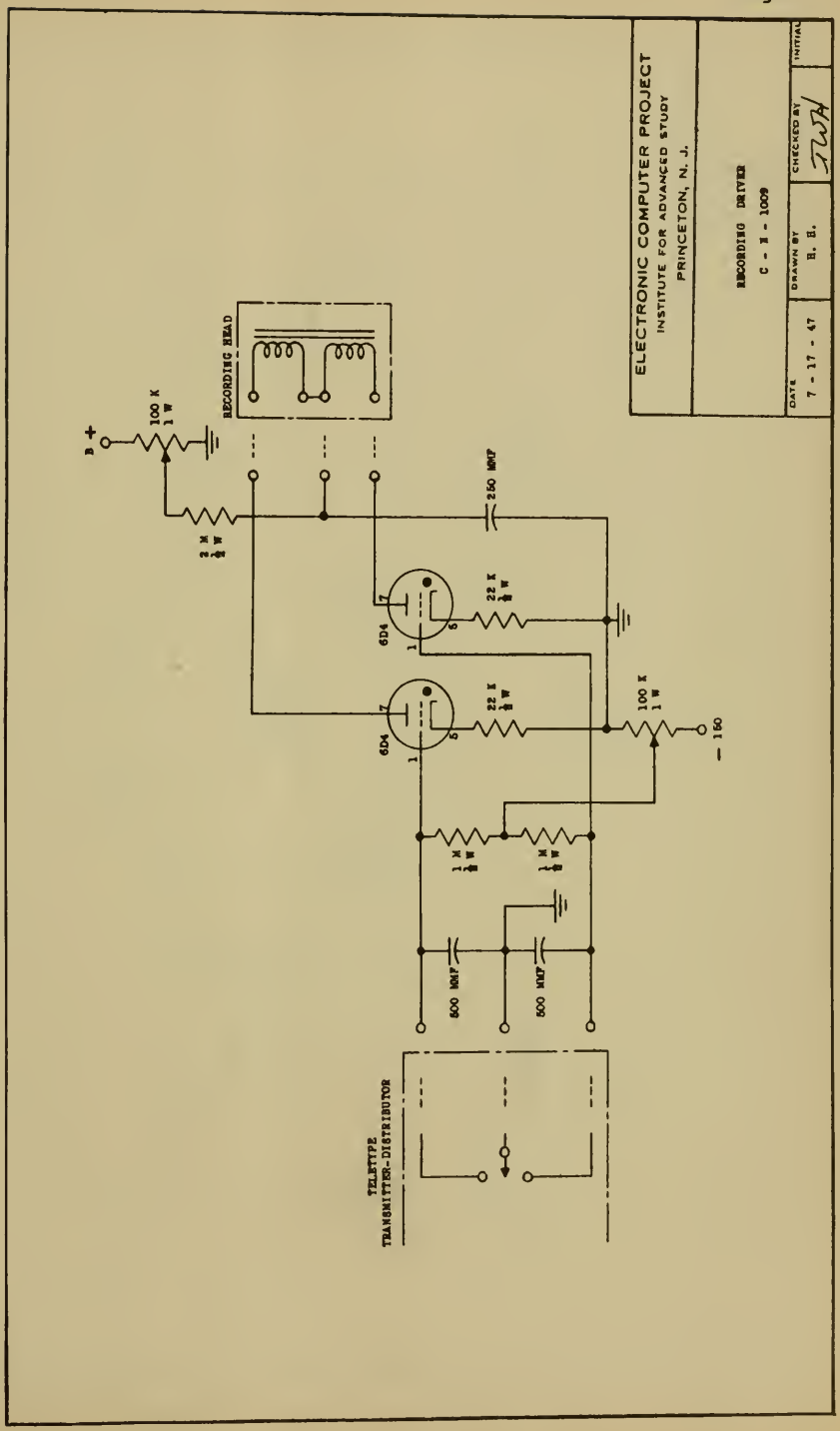


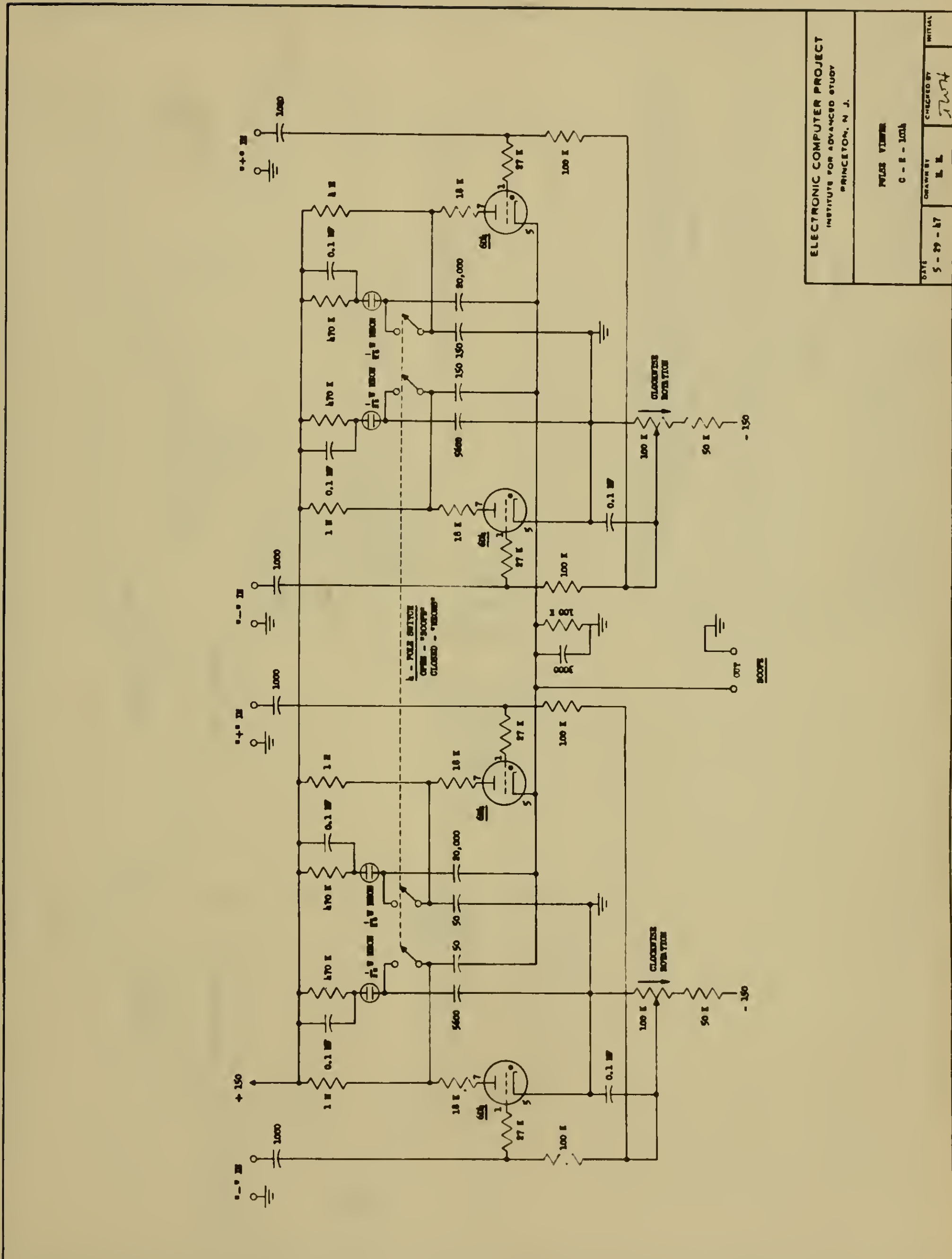
Figure 17
Pulse Limiter

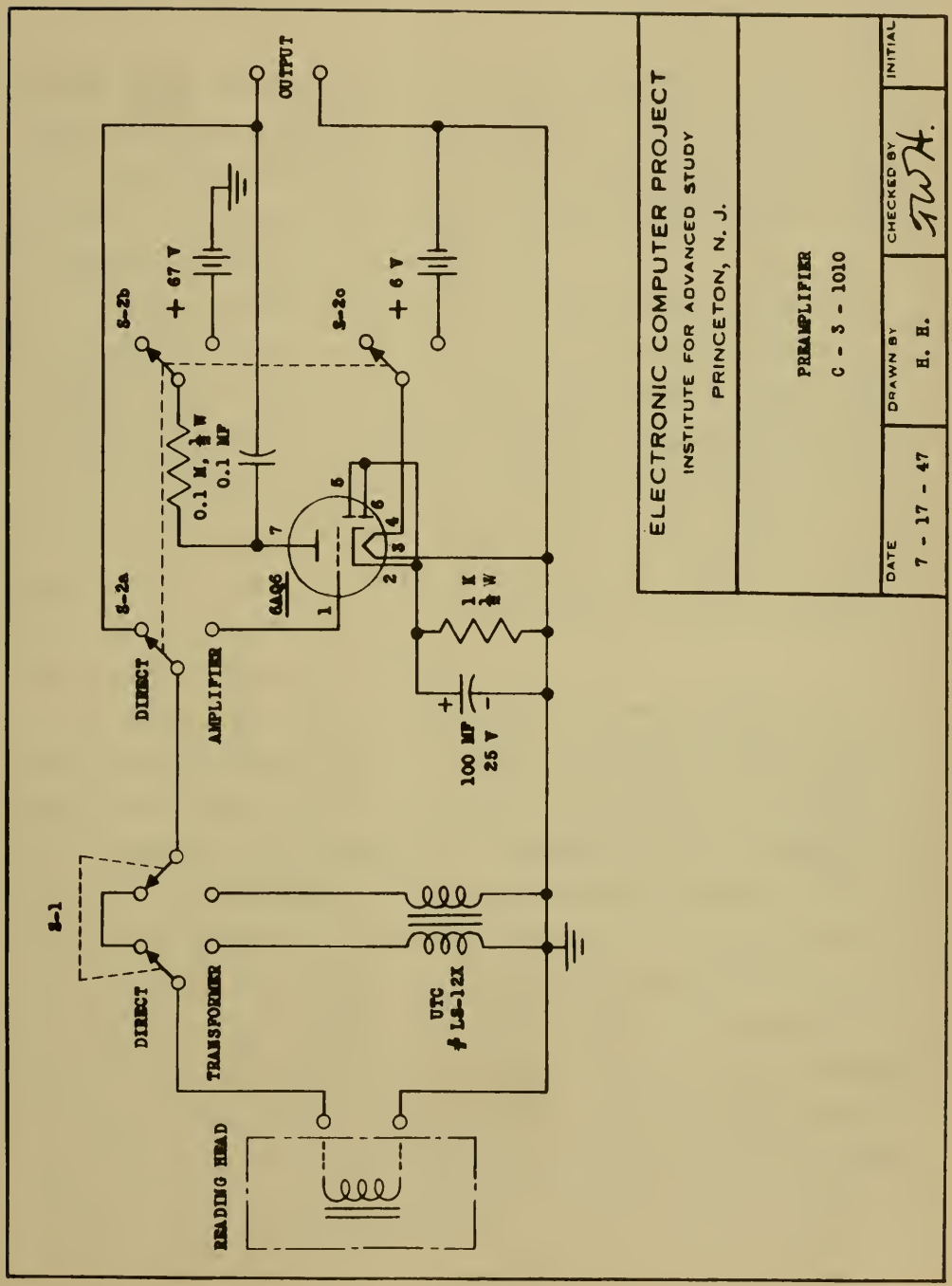
Figure 16
Voltage Pre-amplifier

Figure 19
Pulse Selector

Figure 18
Pulse Shaper


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
RECORDING DRIVER
C - I - 1009
DATE
7 - 17 - 47
DRAWN BY
H. H.
CHECKED BY
INITIAL
+ B
100 K 1 W
RECORDING HEAD
2 K 1 W
250 MMF
6D4
22 K 1 W
100 K 1 W
- 150
1 K 1 W
800 MMF
TELETYPE TRANSMITTER-DISTRIBUTOR


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
DATE
5 - 29 - 47
DRAWN BY
CHECKED BY
INITIAL
+ 150
- 150
1000
27 K
18 K
100 K
50 K
470 K
1 M
0.1 MF
20,000
5600
150
50
OUT
SCOPE


OUTPUT
+ 67 V
+ 6 V
S-2b
S-2a
S-2c
0.1 M, ½ W
0.1 MF
6AQ6
1 K ½ W
100 MF 25 V
DIRECT
AMPLIFIER
S-1
DIRECT
TRANSFORMER
UTC # LS-12X
READING HEAD
ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
PREAMPLIFIER
C - 3 - 1010
DATE
7 - 17 - 47
DRAWN BY
H. H.
CHECKED BY
INITIAL

G.R. 714A voltage amplifier; thereafter the amplified pulses to a "pulse limiter" (9) which standardizes the pulse amplitude. As may be seen by inspection of diagram C-3-1003 this circuit consists of a pair of double triode gates, arranged so that incoming pulses of either polarity merely allow or deny passage of a standard output current. (See Figure 17.)

Emerging from the pulse limiter the information passes to Step 10 the "pulse shaper" (Figure 18) which may be seen by inspection of diagram C-3-1005 to consist essentially of two toggle circuits having a "normal" state and arranged to be tripped to the "abnormal" state by a positive pulse in one case, and by a negative pulse in the other; the recovery time being set by an R-C time constant. The input being sensitive compared to pulse amplitudes normally received, and the transition of the toggle being relatively sharp, and the recovery time-constant stable, it is seen that this device produces an output uniform in duration and amplitude.

The next step (11) is designated "Pulse Selector", (Figure 19) the effect desired is essentially that of producing well-behaved unidirectional pulses corresponding to the + -, and - + voltage pairs relayed by the pick up head in consequence of differentiation of the magnetic signals signifying "1" and "0". This requirement of inverting a differential operation calls for a process essentially in the nature of integration; however, as a result of the special form of the signal originally recorded, whereby all information is confined to the unique property of binariness, it may be shown that the process of integration degenerates into a matter of counting, and of reproducing the information in regularized binary form. This may be realized by various contrivances according to fancy; a simple representative being that represented in diagram C-3-1004 entitled"Pulse Selector". This circuit is arranged to

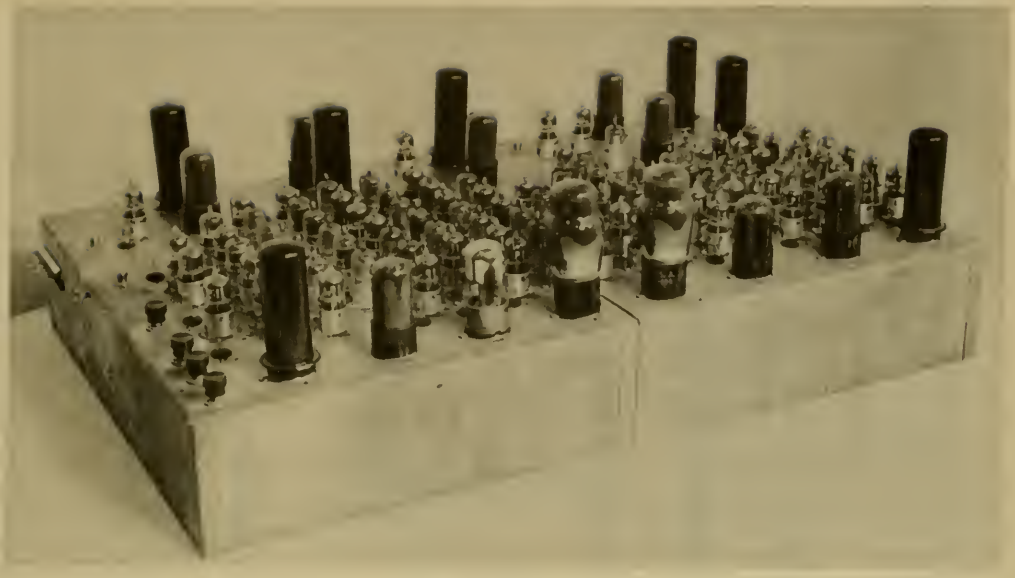


Figure 20
Indexer-Interpreter Chassis II

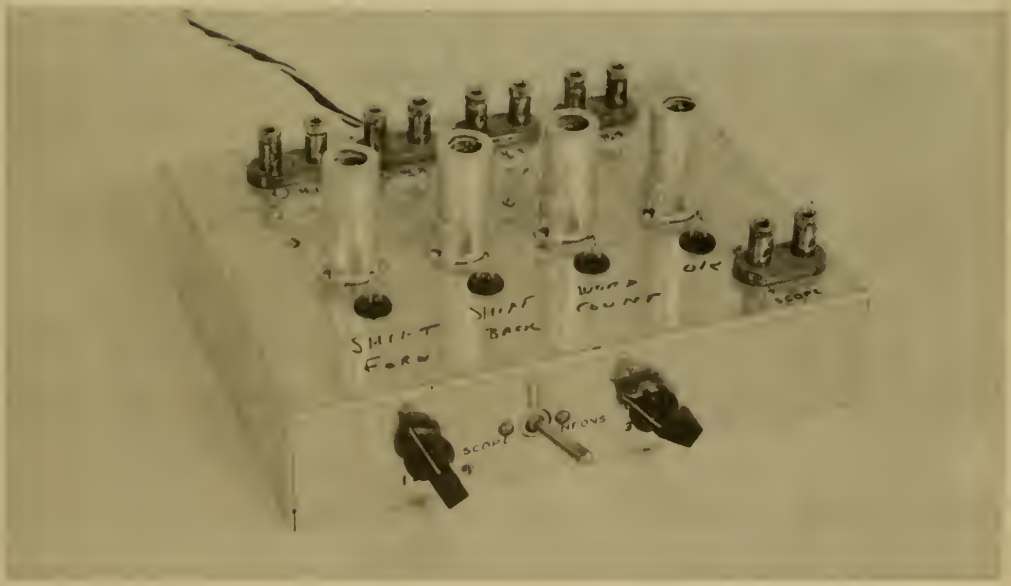
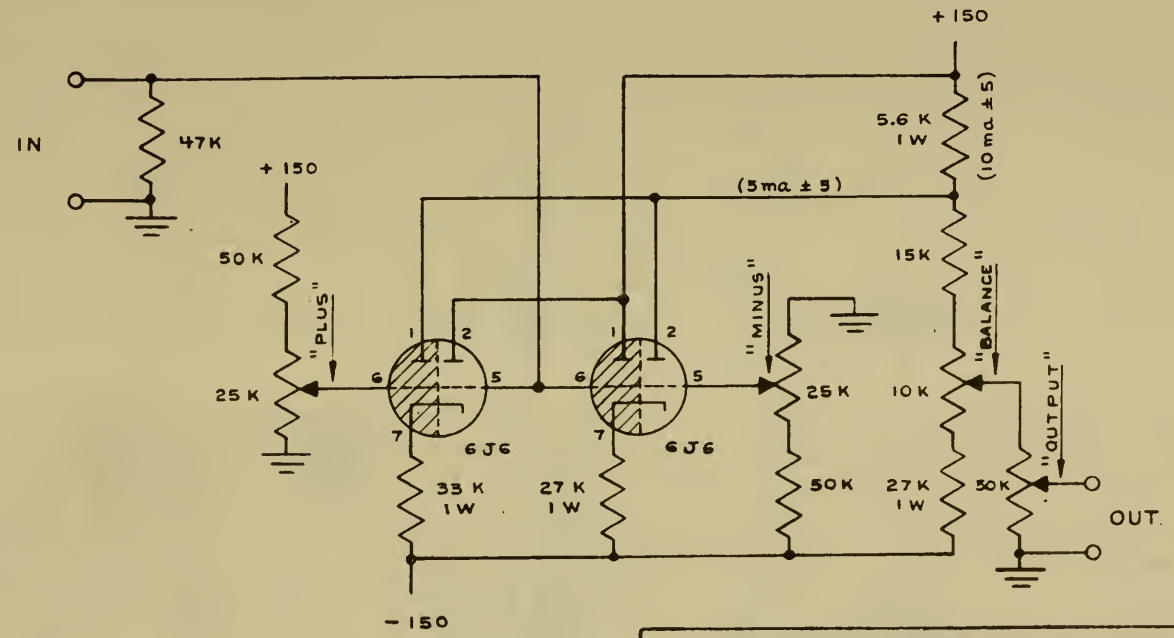


Figure 21
Pulse Viewer



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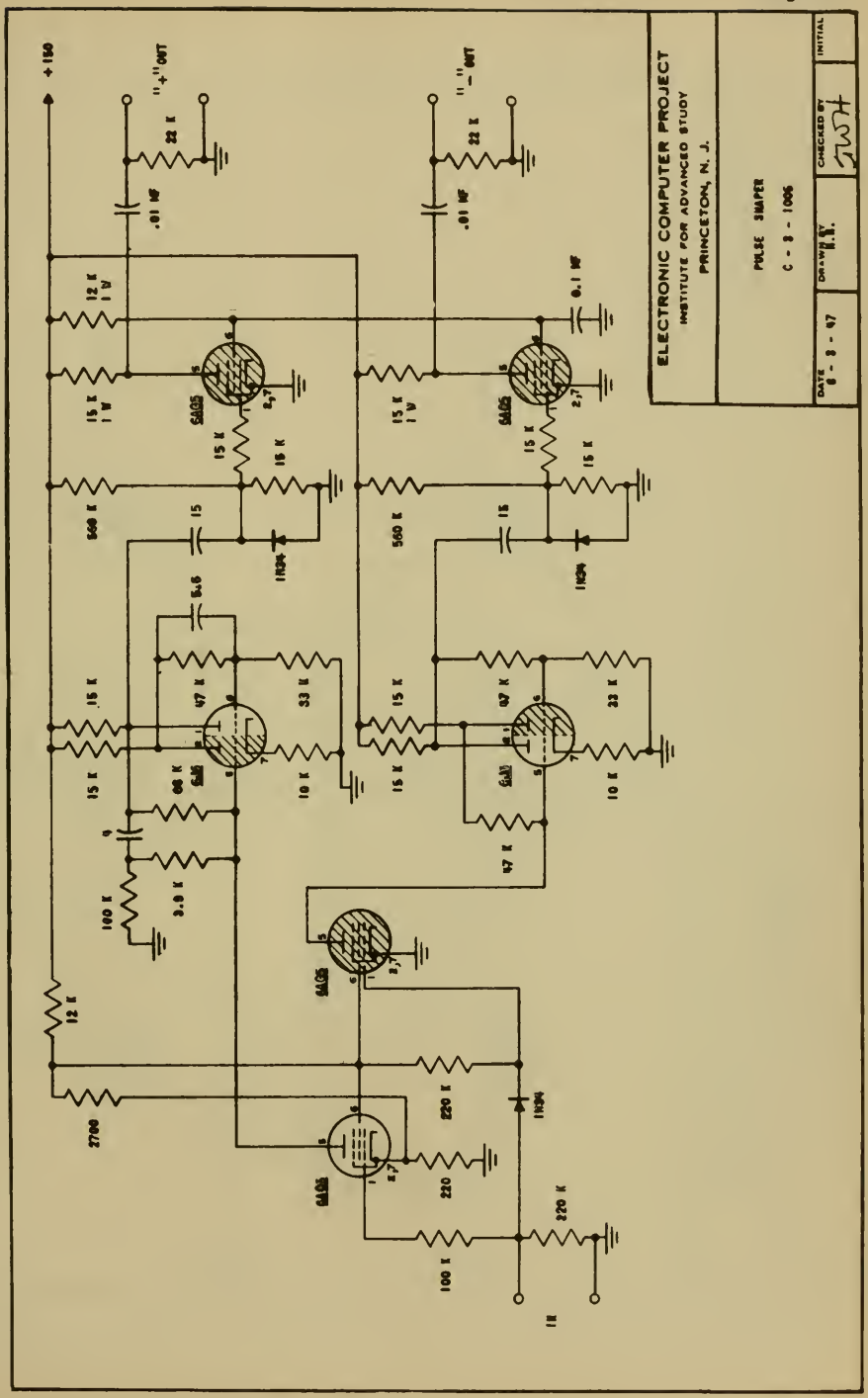
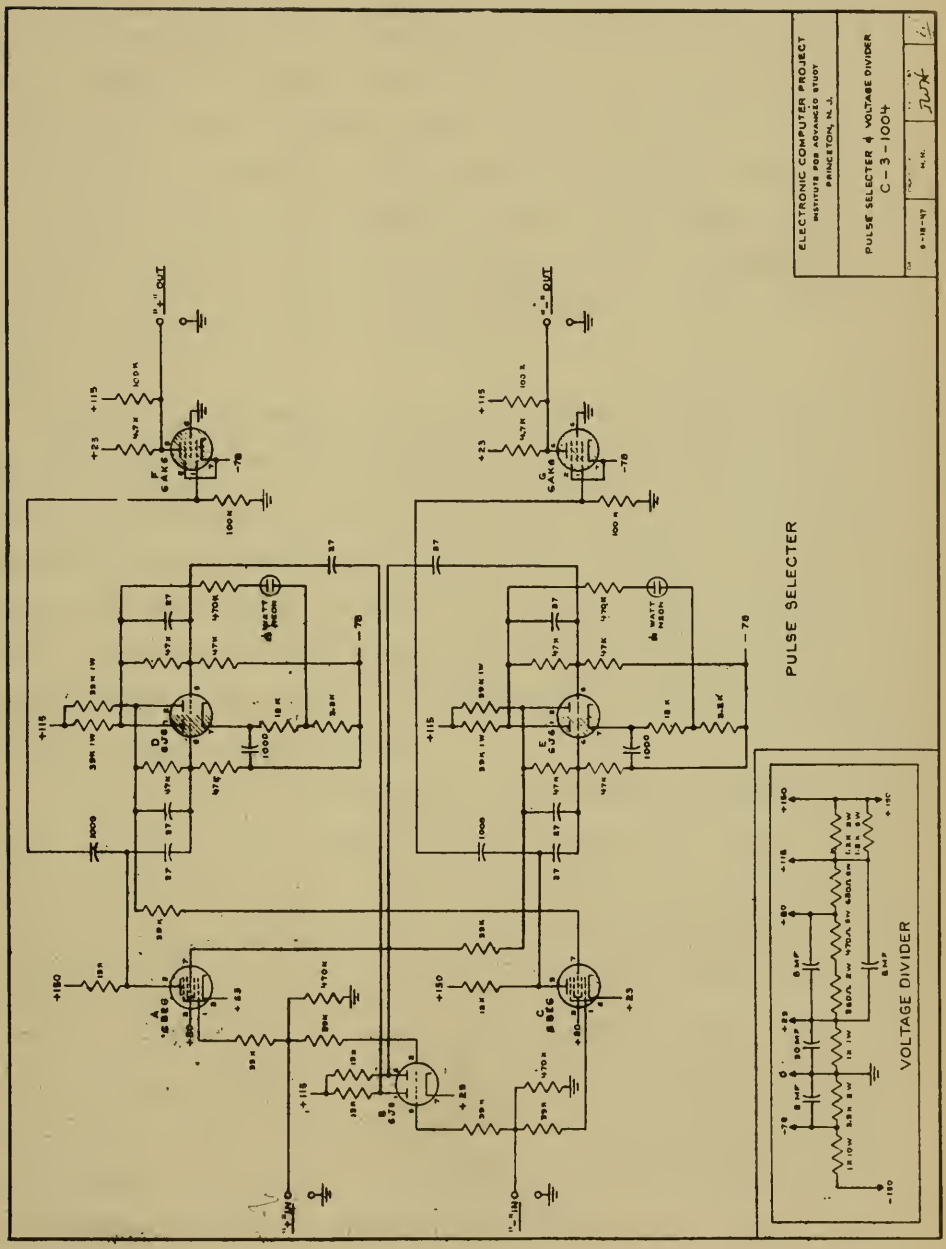
PRINCETON, N. J.

PULSE LIMITER #1
C-3-1003

DATE	DRAWN BY	CHECKED BY	INITIAL
3-26-47	H. H.	RJS	


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
PULSE SHAPER
C - 8 - 1006
DATE 6 - 8 - 47
DRAWN E.T.
CHECKED BY
INITIAL
+150
"+" OUT
"-" OUT
.01 MF
22 K
12 K 1 W
15 K 1 W
6AQ5
2.7
15 K
560 K
15
1N34
5.6
47 K
33 K
10 K
6AL5
68 K
100 K
3.9 K
2700
220 K
220
100 K
0.1 MF


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
PULSE SELECTER & VOLTAGE DIVIDER
C-3-1004
PULSE SELECTER
VOLTAGE DIVIDER

receive the differentiated pulse pairs and to transmit only the first, deleting the second; subject to the condition that if two pulses of like polarity occur in succession, the circuit will reset so as to identify the second of the twins as the first pulse of a normal pair, and thereafter to delete the second. The circuit consists of two pairs of toggles, each having a normal state and an abnormal state to which it is driven upon receipt of a pulse of appropriate sign, and each arranged to inhibit the operation of the other until restored to normal.

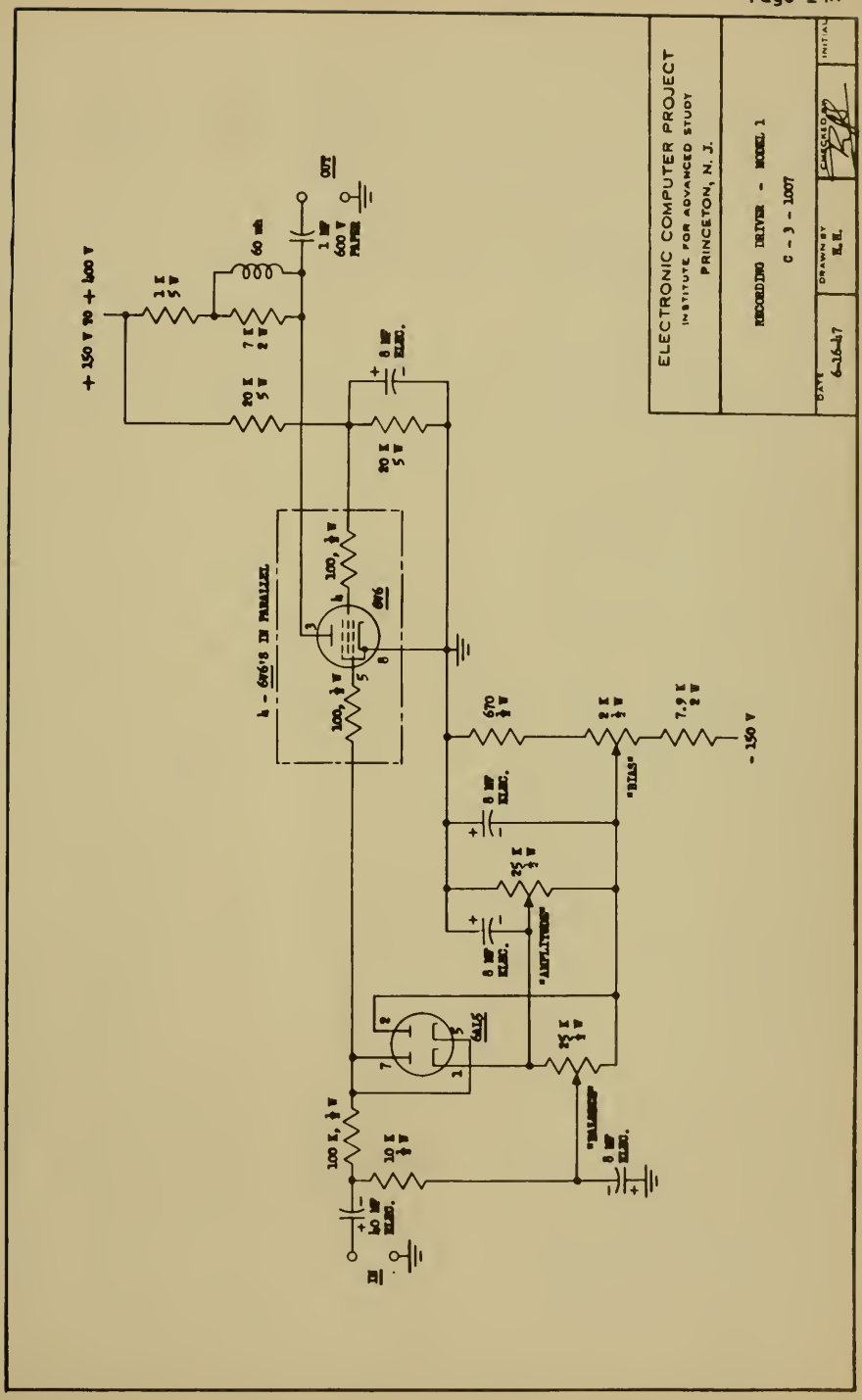
Finally, the information proceeds to the indexer-interpreter (step 12, Figure 15) where markers and word end signals are identified, verified and deleted, and the information forwarded to the shifting register. The operation of this component was discussed in some detail in P.R. 1 and need not be developed further here, except to remark that with the completion and tests of chassis II, (Figure 20) the chain of high speed input components has been completely constructed and tested, and may be considered suitable for operation in the primitive model computing machine.

Emerging from the index-interpreter, the information proceeds to the shifting register (13) and thence to the inner memory (14). Several satisfactory shifting registers have been built and will be described later in this report. In conjunction with the operation of installing data into the shifting register from the Indexer-Interpreter, a control function must be provided to pulse the shifting register, thus commanding "shift" at the incidence of each datum, and causing transfer to the selectron memory M-1 after each word. Pulsers suitable for this have been developed and will be described later in this report; at present these are being arranged with suitable gates to carry out the sequence of operations.

The "output" or read out operation may now be considered, and since this includes many steps duplicating those already described some abbreviation is possible. The first step is to transfer data from the inner memory to the shifting register in parallel, and then read-out serially from the shifting register. As this is accomplished by shifting the register, markers and word-end groups must be introduced as indicated by step 15, "Encoder". This step consists essentially of a control and counting operation, and the problem is now being studied with a view toward carrying it out through modifications of the existing "indexer-interpreter" (12). It may be noted in passing that since the shift operation of the register, and associated gating operations can be accomplished at electronic (microsecond) speeds, this operation and the marker insertion may be temporally enslaved to the read-out high speed wire drive, so as to minimize the inconvenience resulting from dynamics. Thus, the wire drive may accelerate, run at non-critical high speed, and stop in any fashion and yet receive pulses of even spacing on the wire.

Emerging from the encoder, the pulse data passes to a recording head driver amplifier (step 16) designated Mod 1 and diagrammed in C-3-1007 where it will be seen to consist of a parallel arrangement of heavy current power amplifier tubes (4 type 6V6) coupled by L-C elements to the recording head. The circuit has been arranged to handle pulses of either sign, and is equipped with a high-gain pulse shaping amplifier on the input. This arrangement drives the recording head, over which the magnetic wire is traversed by a high speed drive as discussed in connection with the input sequence.

Thereafter the low speed output sequence assumes the data; proceeding from a low speed wire drive and pick up head (18/17) to a high gain voltage amplifier (19), through limiting, shaping and selecting circuits (20-22) to an interpreting circuit (23) associated with the tape punch (24) and then via tape


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
RECORDING DRIVER - MODEL 1
C - 3 - 1007
DATE
6-16-47
DRAWN BY
R.E.
CHECKED
INITIAL
+ 150 V to + 400 V
OUT
60 mh
1 MF
600 V
PAPER
2 K
5 W
7 K
2 W
20 K
5 W
0.1 MF
ELEC.
100, 1 W
6V6
1 - 6V6's IN PARALLEL
670
1 W
2.2 K
1 W
7.9 K
2 W
- 150 V
"BIAS"
0.1 MF
ELEC.
25 K
1 W
"AMPLITUDE"
6SL7
100 K, 1 W
10 K
1 W
"BALANCE"
50 MF
ELEC.
IN

to the teletype transmitter. This sequence of operations is to be accomplished by apparatus to be delivered by the Bureau of Standards; meanwhile by connecting units which we have already constructed (and described above) it is possible to feed information in fashion adequate for temporary tests from slow speed wire drive to tape punch to teletype printer.

Finally Figure 22 presents a view of the entire input system mounted on a standard rack-and-panel arrangement suitable for test operation.

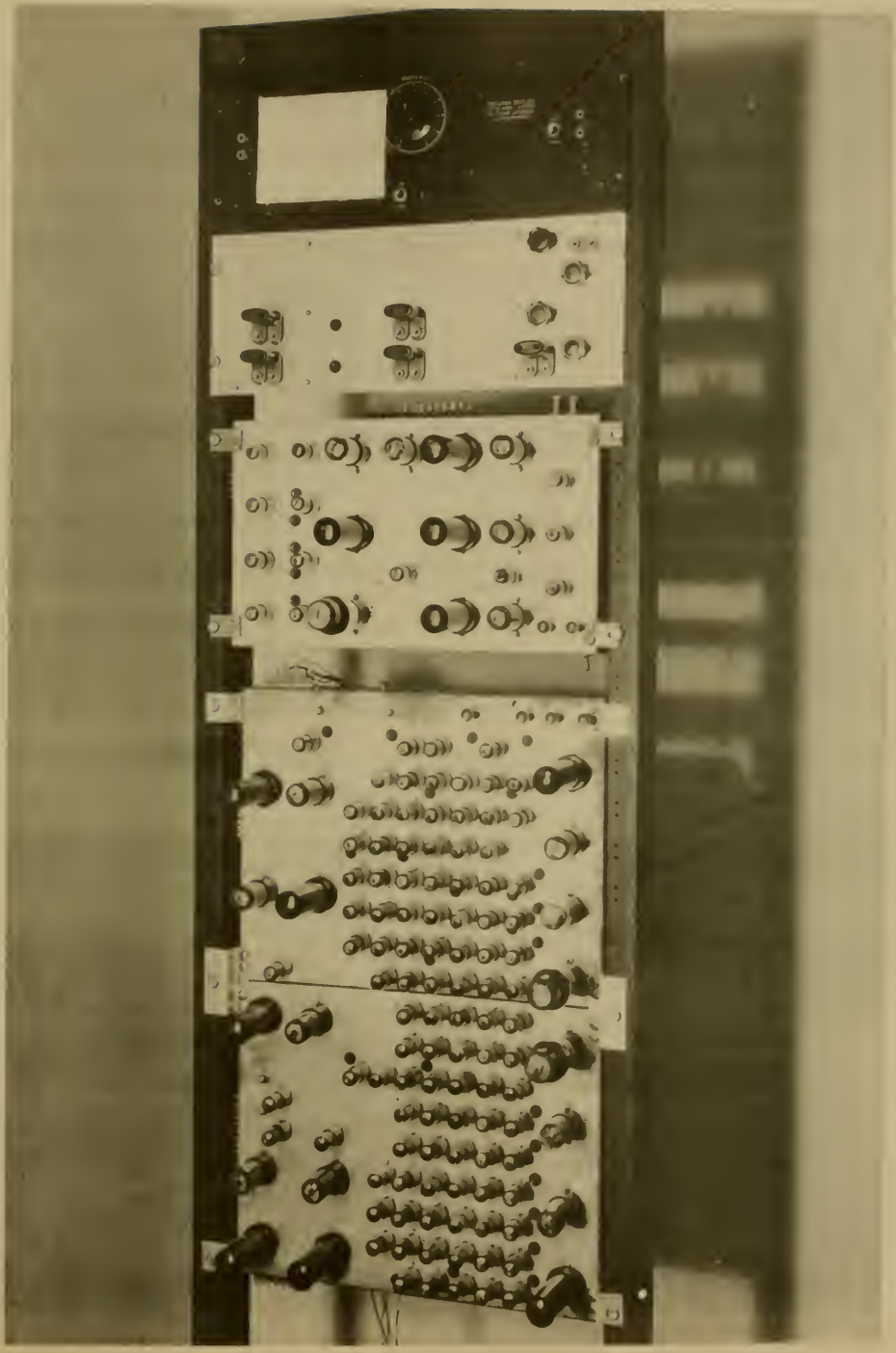


Figure 22
Input Circuits

VIII. BINARY ELEMENTS: TEST APPARATUS

In addition to various elements, components and organs the development of which are essential to effect operations proper to the computing machine (discussed in earlier and later sections of this report), it invariably becomes expedient or necessary to evolve devices of an auxiliary nature, such as test equipment, oscilloscope accessories, etc. In this section a few of these will be mentioned briefly.

(1) Register and accumulator components of the arithmetic organ exchange their information normally in parallel fashion, each of forty cells receiving from, or discharging into a corresponding cell. In certain schemes for designing such registor or accumulator components coupling devices or gating circuits are used for the parallel transfer which include essential time-constants; that is, they are pulse-actuated. (See discussion of Section 10, this report.) Accordingly, it becomes convenient for test purposes to have a manually initiated device capable of issuing an optional combination of pulses on many parallel channels each time a push-button is operated, so that representative test-words can be transferred into such a pulse actuated register or accumulator. Figure 24 is a diagram of such a device, and consists simply of a single thyratron pulser with choice of recovery time-constants (.1, .2, and .4 microseconds) arranged in conjunction with a ganged, manually operated switch. Figure 23 shows realization of this device inten stages.

(2) In constructing many types of experimental circuits time is lost and circuit parts rendered unfit for further use by the usual practice of punching and assembling special chassis, soldering pigtail resistors and other elements to terminal lugs and to each other, etc. It has been found

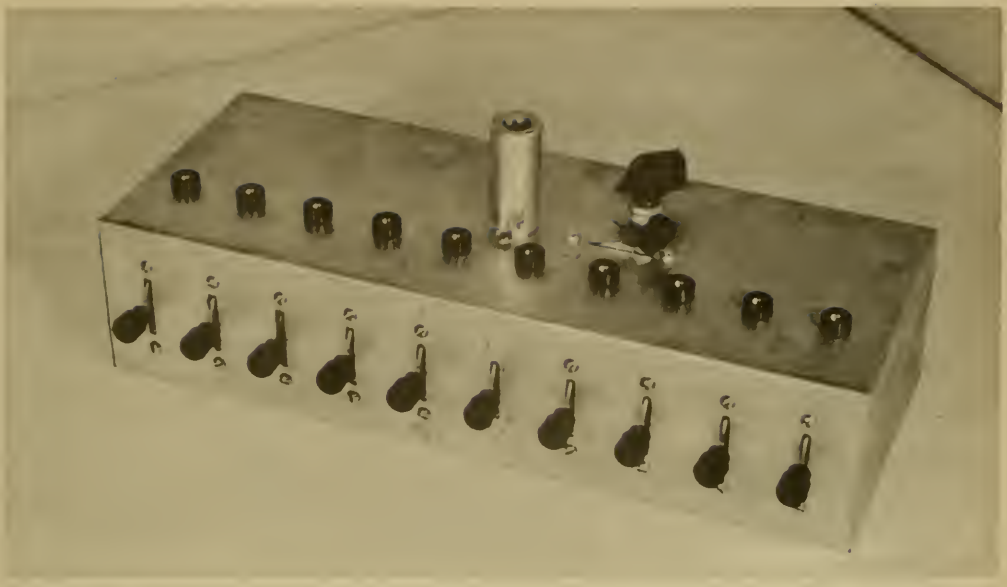


Figure 23
Ten Output Pulse Generator, Chassis

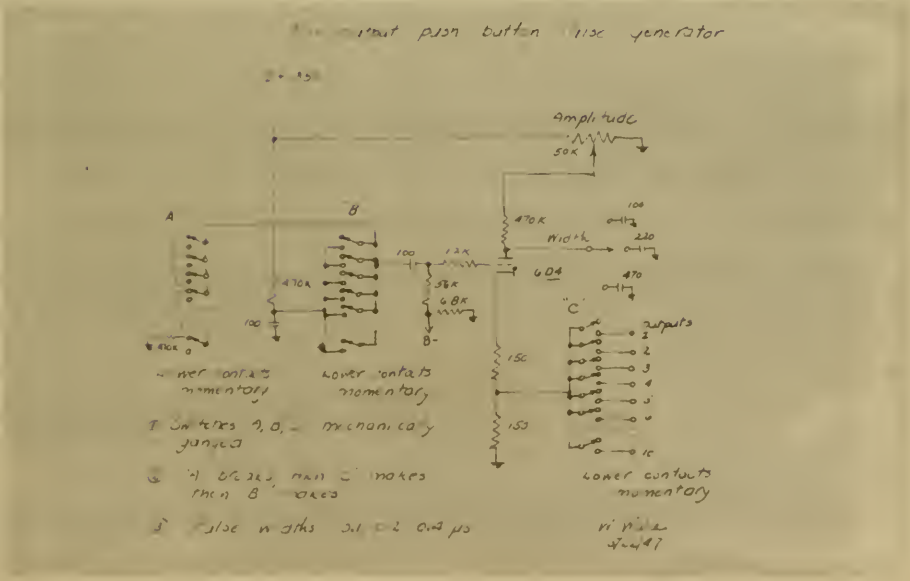


Figure 24
Ten Output Pulse Generator, Diagram

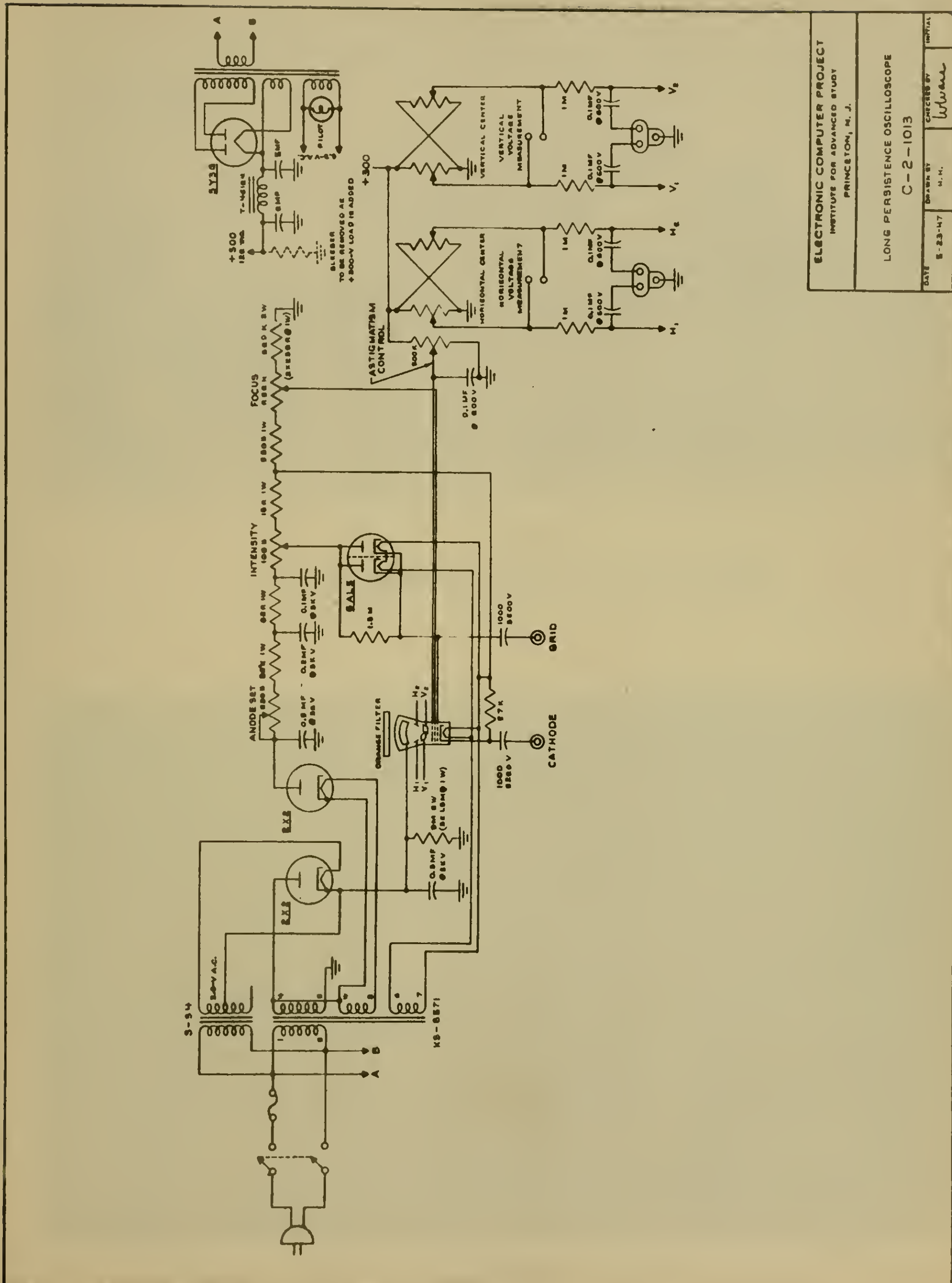
convenient and economical of time and experimental parts to provide several standard experimental chasses fitted with a suitable number of tube sockets and a rather extensive array of independent, permanently mounted bus-bars. With this arrangement it is often possible to assemble an entire test circuit of several tubes without bending, clipping or entwining the pigtail of a single resistor, condenser or other element. A circuit of this sort can be assembled in very short time, and any part replaced with another almost immediately; furthermore, when the job is over, parts can be salvaged undamaged. This arrangement is shown in Figure 30.

(3) For viewing single trace transients of low repetition rate - such as the effect of splices in the magnetic wire - a small long-persistence oscilloscope was constructed, and a circuit developed suitable for single-trace transients. This is pictured in Figure 31 and the circuit in diagram C-2-1013.

(4) For various test purposes it is convenient to have a means of indicating pulse repetition rates (as when reading data from magnetized wire drivers at a speed not known to be constant). Accordingly a simple rate indicator was devised covering the frequencies 0 to 20 KC in three ranges. This device is pictured in Figure 32 and consists essentially of a triggered circuit, the output of which is accumulated, averaged and read on a milliammeter.

(5) In order to study pulses of high amplitude and high (megacycle) repetition rates such as are produced by blocking oscillators, on a cathode ray tube, it is desirable to have means for triggering the sweep at each "N th" pulse rather than to attempt use of the ordinary saw tooth sweep. This is because with the usual sawtooth sweep, an aribitrary sweep length cannot be used independently of the locking frequency.

Accordingly means is required which will actuate a "triggered sweep" (ordinarily capable of about 5000 c.p.s. repetition rate) at every "N th"


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
LONG PERSISTENCE OSCILLOSCOPE
C-2-1013
DATE 5-23-47
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HORIZONTAL VOLTAGE MEASUREMENT
+300
KS-8571
5Y3G
2X2
2X2
PILOT

Figure 27
Variable Parameter Megacycle Pulse Generator

Figure 28
Variable Parameter Megacycle Pulse Generator Performance
Duration - 2.3 to .2 microseconds
Amplitude - 0-80 volts
Rise and Fall (10% to 90%) - about .1 microsecond

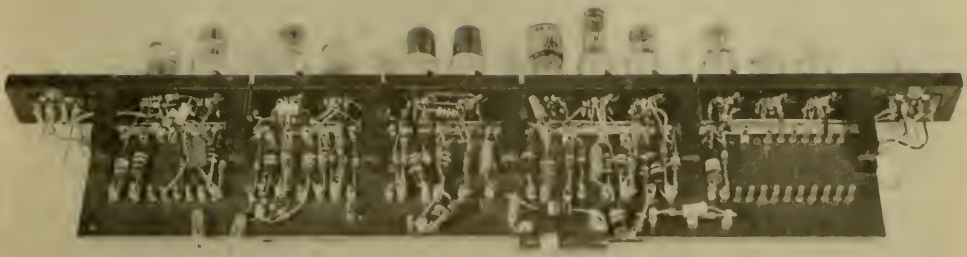


Figure 29
Single Channel of Accumulator Component

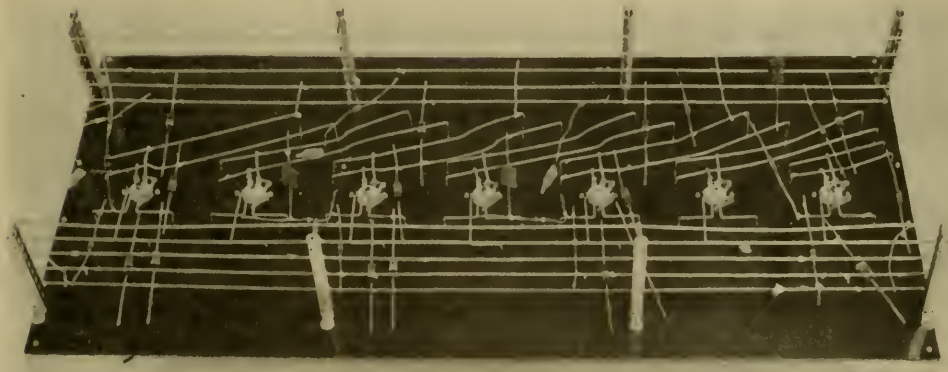


Figure 30
Chassis for Experimental Circuits

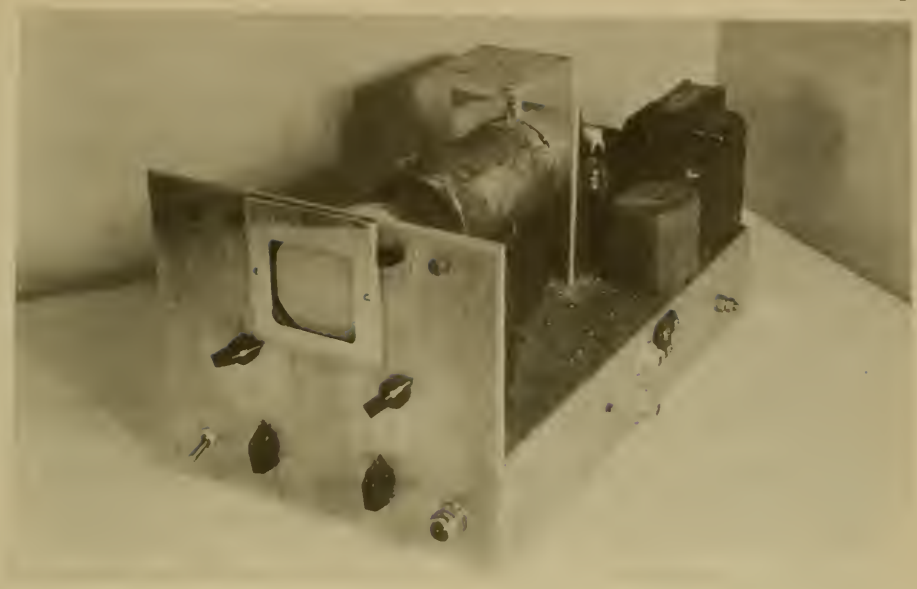


Figure 31
Single-Trace Long Persistence C.R.O.

Figure 32
Pulse Repetition Rate Indicator

pulse where N is on the order of 200. The conventional approach to this problem would involve "scaling down" in frequency by harmonic submultiples; a technique which is manageable only in steps of a decade or less, so that about three stages would be needed. Further, in dealing with pulses any such "scaling down" is a tenuous process because the non-linear shock-excited character of the pulses causes them to vary in minute detail from pulse to pulse, so that any scheme of locking with them is apt to "jitter" due to random irregularities in the locking point.

This difficulty may be overcome by the stratagem of operating a gate so as to bracket every N th pulse by a safe margin, allowing this pulse itself to pass and trigger the sweep. The details of this scheme may be gathered from inspection of Figure 6E and circuit C-2-1016.

Actually, the submultiplying oscillator is allowed to trigger on every "N th" pulse according to the usual relaxation scheme, and the "jittery" pulse so obtained is arranged to open a gate bracketing and passing the N+1 th input pulse, which is consistent in location. The device operates well on inputs from 10 KC to about 1.8 megacycles provided the amplitude exceeds about 10 volts. The triggoring pulse produced is on the order of 5 KC and varies in time by less than .025 microseconds. The outfit is pictured in Figure 26, and entitled "Pulse Synchronizer".

(6) For purposes of testing arithmetic components and control elements, as when a shifting register is called upon to shift, then transfer, in rapid succession, it is convenient to have available a pair of very narrow, controllable, high energy pulses. These may be obtained from the "sliding multiple pulses" described in section 8.6 of P.R.1. However, the pulses so produced are of steep front but of exponential decline, so that they are sharp

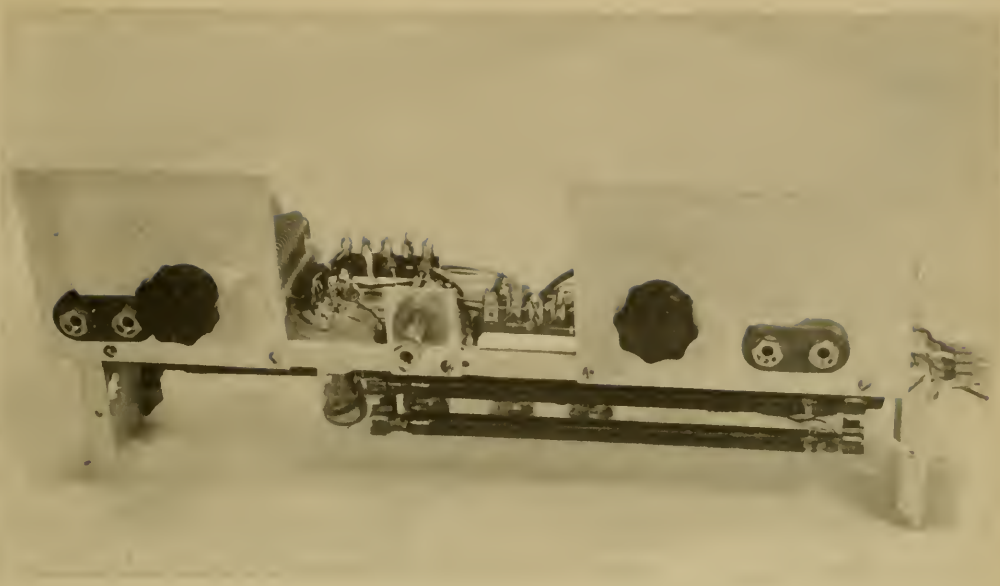


Figure 25
Dual Whisker Generator

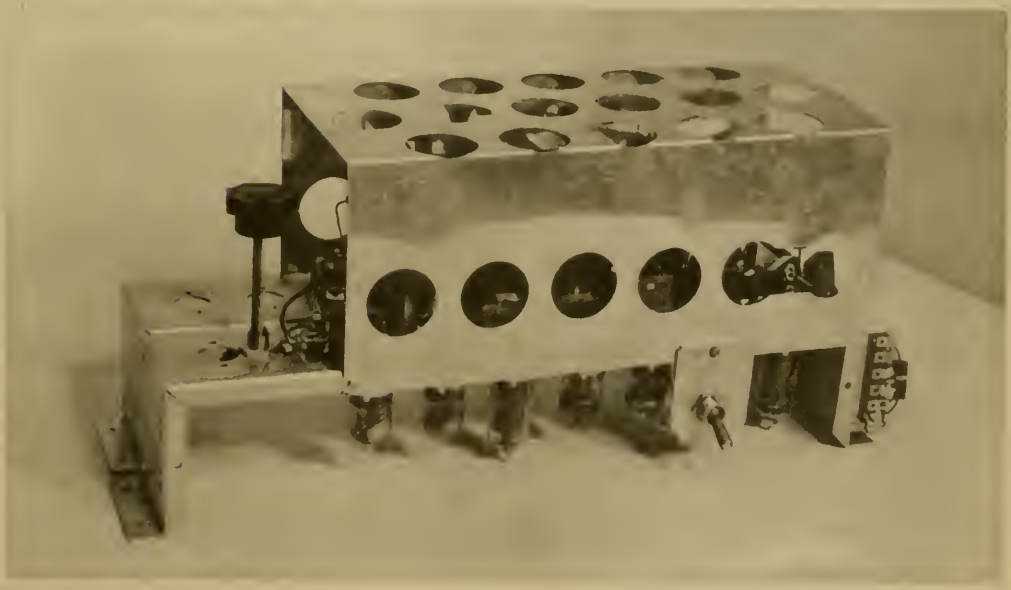
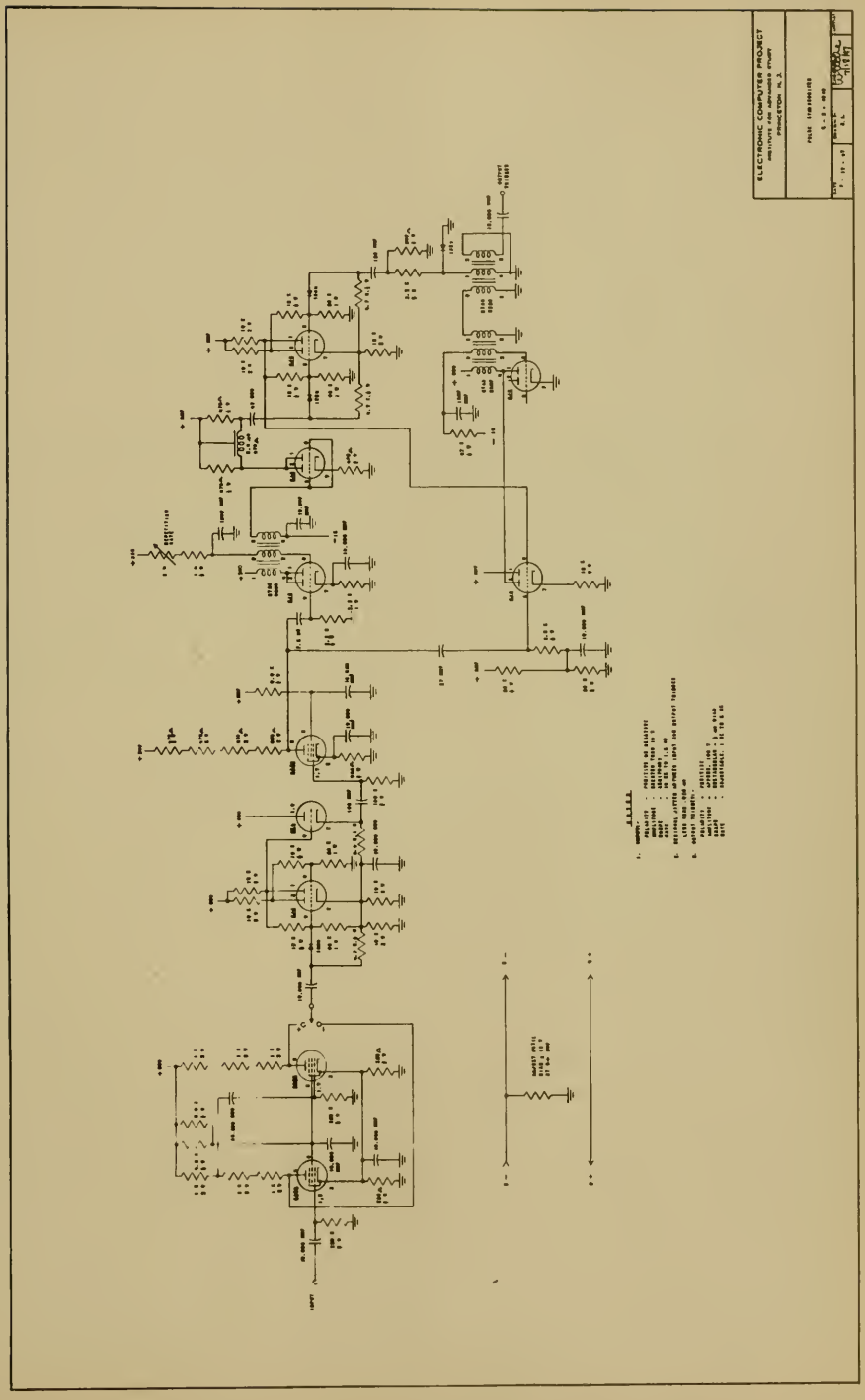
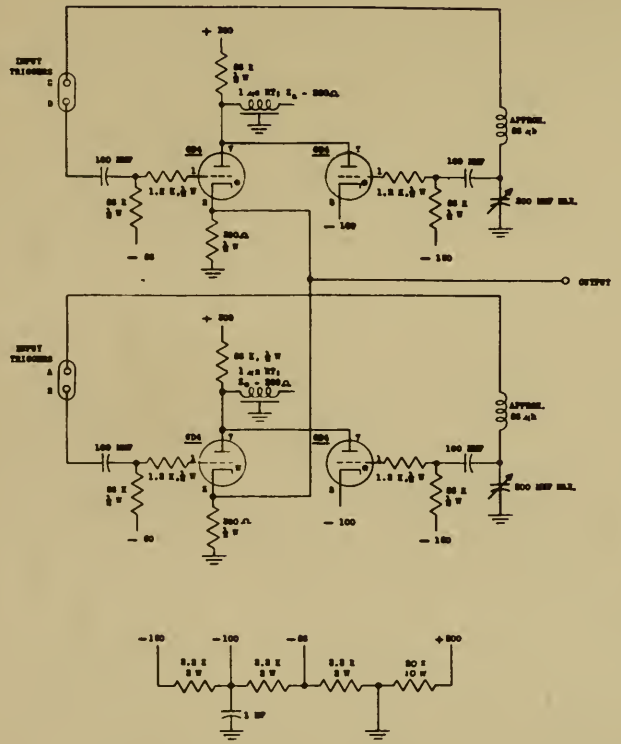


Figure 26
Pulse Synchronizer



topped and broad at the base. Square topped pulses of equally sharp rise and fall are more desirable in many cases, and the circuit of diagram C-2-1018 was developed for such test purposes; and built in the form pictured in Figure 25 "Dual Whisker Generator". This device consists essentially of two independent circuits, alike in every respect, consisting each of a pair of thyratrons arranged to fire in succession, causing a sharp rise and sharp fall in voltage output.

Each such twin thyratron circuit is initiated by a pulse from the sliding pulser (P.R.1 - 8.6) so that their proximity is continuously adjustable; and each circuit has a rise and a fall time of about .015 microsecond; the intervening dwell being adjustable from .2 microseconds to about .05 microsecond. The output pulses are 100 volts in amplitude and the equivalent source impedance is about 180 ohms.

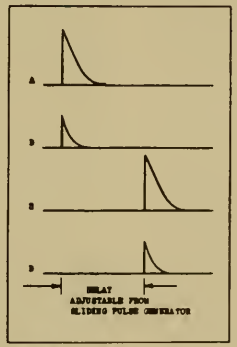


NOTES

1. INPUT TRIGGERS

   a. A AND D, MAINTAIN OUTPUT OF SLIDING PULSE GENERATOR; B AND D, ADJUSTABLE OUTPUT OF SLIDING PULSE GENERATOR.

   b. A AND B COINCIDENT; C AND D COINCIDENT.



   c. ALL TRIGGERS 0.1 μs WIDE.

2. OUTPUT PULSE

   a. WIDTH APPROXIMATELY .04 μs TO 0.2 μs.

   b. AMPLITUDE APPROXIMATELY 100 V.

   c. SHAPE RECTANGULAR - RISE TIME .01 μs; - FALL TIME .01 μs.

   d. PULLING BETWEEN OUTPUT PULSES NEGLIGIBLE.

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IX. BINARY ELEMENT PERFORMANCE STUDIES

The program of development between 1 January and 30 June 1947 has not emphasized research on binary elements. The program has rather been directed toward composing the best possible computing machine using binary elements of about the state of development reported in P.R. 1; holding in abeyance the question of more refined analysis and design until the time arrives to perfect the "primitive model" computer and convert it to a complete and automatic version.

However, a few advances have been made which have facilitated design of register and accumulator components as discussed in sections 10 and 11 of this report. These advances will be discussed briefly at this point and more completely at a later time.

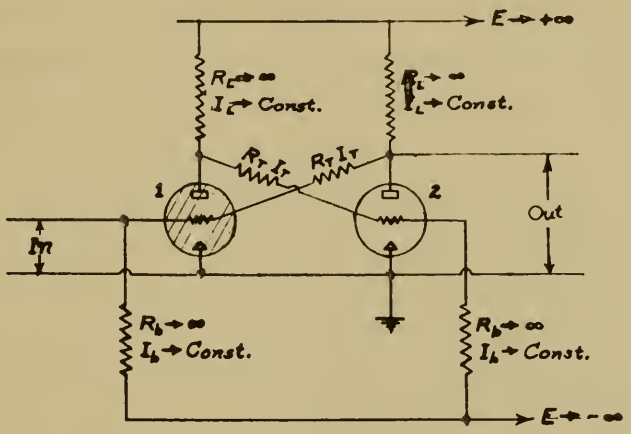
(1) Concerning the ratio of input to output energy sensitivity in a toggle circuit. For circuits of the "direct, locked transfer" type, such as discussed in P.R. 1 and in section 10 to follow, the object is to transfer energy from one toggle-cell to another by gate-connecting the output of one to the input of the other (P.R.1, section 9.53). Which way the information goes depends upon the relative sensitivity of the input and output; and if the input is a great deal more sensitive - that is, if for less energy transfer is required to shift a toggle when acting on the input as compared to that needed to effect the output, then direct locked transfer of the desired sort can be effected quickly and with certainty.

To study this sensitivity ratio it has been found convenient to consider a standard toggle circuit in which the resistors and bias voltage are allowed to assume extreme values, so as to minimize the undesirable losses of transfer energy due to attenuation in the resistor network. Referring to

Figure 33 it may be seen that this is accomplished by allowing the load resistors R_L and the bias resistors R_B to approach infinity and also to make the positive (E+) and negative (E-) voltage supplies approach infinity. The result is quite interesting: The bias current I_B and the load current I_L become constants, so that the loss of transfer energy due to the resistor network is indeed minimized. However, it is trivial to show that the grid current in the "on" tube is now exactly equal to the plate current, and in fact that the ratio between input and output currents to effect a transfer of state is now exactly unity. Clearly this results from the fact that the only limit to the positive plate excursion of the off tube is the grid current drawn at the "on" tube.

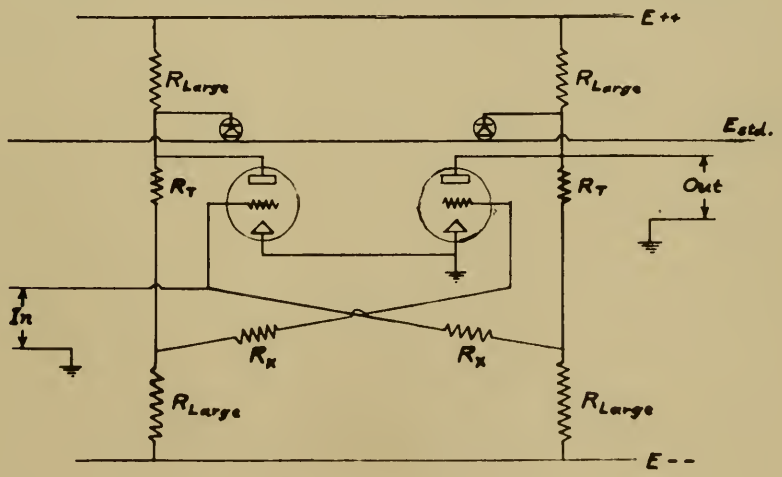
This example clearly indicates the incompatibility of the conditions desired in a standard toggle circuit. If the pure resistance exterior network is arranged to give maximum locking and transfer gain between tubes, the sensitivity ratio approaches unity whereas if the resistors and voltages be adjusted to minimize the grid current in the "on" tube, the attenuation is high, the transition is weak instead of sharp, and the"locking" weak and of uncertain swing.

These counteractions may be avoided by re-designing the toggle network as indicated in Figure 34. Here R_L and R_B as well as E+and E- are allowed to be very large, so that the load and bias currents are nearly constant. However, the positive swing of the off plate is limited by a crystal rectifier to a predetermined standard voltage. The transition resistor R_T is chosen at will, and gives in effect a constant voltage drop. The grids are connected to the transposition points via a new resistor R_X the value of which may be selected at will, and can be of any value from zero to several megohms. The current sensitivity of the circuit is now adjustable at will by simply choosing



Binary Toggle - Degenerate

Fig. 33



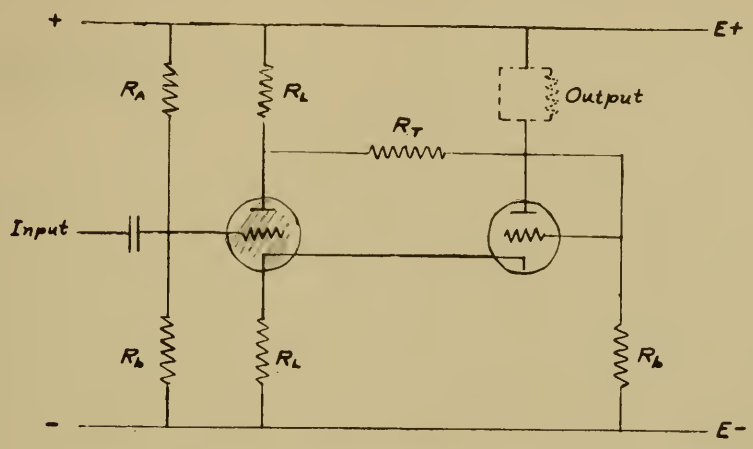
Binary Toggle: Arbitrary Sensitivity Ratio

Fig. 34

R_X. The plate sensitivity is fixed and constant; the crystal must be relieved of the entire plate current load before any plate swing can be effected.

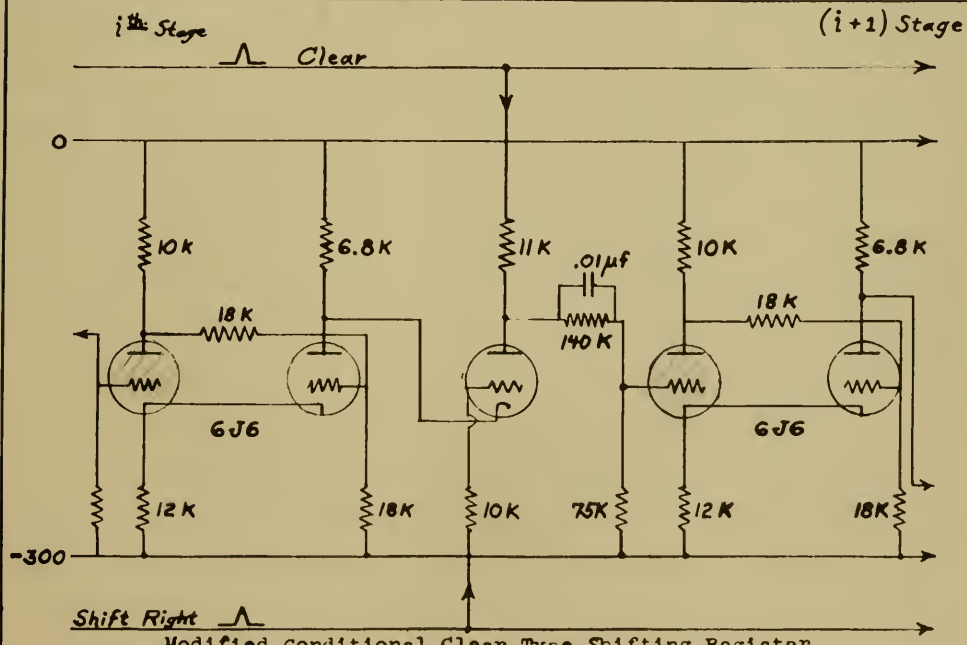
Register circuits using this principle have been designed, built and tested, and are discussed in Section 10 to follow.

(2) Concerning Cathode Coupled Toggles. The nature of the cathode-coupled toggle circuit has already been discussed. (P.R. 1, Section 9.2.) These circuits were found to be greatly improved by increasing the bias resistors (R_B in Figure 36) and voltages in the manner described above. As a result the peformance of the cathode coupled toggle becomes fast and reliable. Futhermore, the cathode coupled toggle possesses a unique property: The input circuit may change state and lock itself securely, even though the output circuit plate be delayed and remain unchanged. This ability permits the input to accept and retain a new state while the output is still at the old state; which adapts the toggle to the design of shifting registers to be described in the next section.



Cathode Coupled Toggle

Fig. 36



Modified Conditional Clear Type Shifting Register
(Shift Left Gates Omitted)

Fig. 37

X. REGISTER COMPONENT STUDIES

(1) Conditional Clear type shifting register.

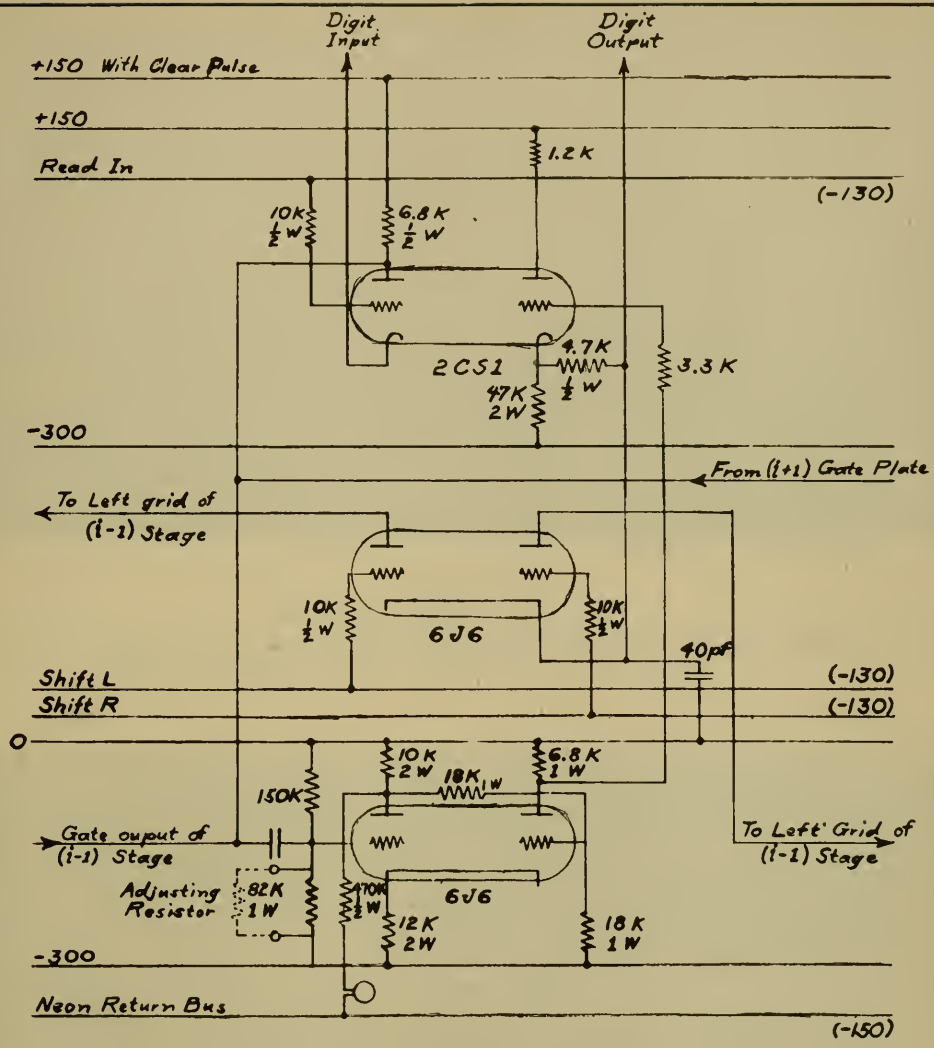
As indicated in the previous discussion, an advantage of the cathode-coupled toggle lies in the ability to lock in either state commanded by the input grid (not cross-connected) relatively independent of the situation at the output plate (not cross-connected). Consequently new data may be arriving and be secured at the input, while previous data is in process of being forwarded at the output, with relatively slight interference between these events.

An example of shifting register circuit utilizing this property is represented in Figure 37. Here a "Modified conditional clear shifting register" is represented by two cathode coupled toggle stages arranged to "shift right" via an interstage triode gate. The cathode of this gate may be swung directly on the output (not cross-connected) plate of the projecting toggle stage, in virtue of the relative independence of the cathode-coupled toggle to output loading, whereas energy from the plate of the shift-gate may be used to drive the recipient toggle grid, via an R.C. delay circuit. The mode of operating this particular circuit consists therefore of simultaneously pulsing the gate grid and the gate plate positive, each via suitable resistors. If the projecting stage contains a zero the gate cathode will be for positive, so that the effect of the positive pulse on the gate grid will be impotent, whereas the "clear" pulse placed on the plate will propagate via the delay to the recipient grid. On the other hand if the projecting toggle contains unity, the gate cathode will be negative and of the two simultaneous pulses that placed on the grid will dominate, causing a negative signal to propagate via the delay circuit to the recipient grid.

A complete shifting register stage designed according to this principle is indicated in Figure 38; this register stage has gates to permit shifting left, shifting right and shifting out (transfer) in parallel. Since three output gates are required for each register stage, the load of their cathodes might overtax the output plate of the projecting stage; accordingly a single stage of cathode-follower power amplification is utilized, raising the total number of triodes per register element to six, contained in three tube envelopes.

The performance of this register appears to be quite acceptable, being able to shift left, right, or to transfer out at a rate of about .6 microsecond. This performance is indicated in oscillograms of Figure 39 and 40. In Figure 39 the upper trajectory represents the pair of pulses commanding shift; the pulses are applied simultaneously to gate grid and plate, but here the grid pulse is inverted to make it visible. The lower traces of Figure 39 show the time of reaction of a receiving stage to these pulses, in the event of propagating a zero and a Unity datum. Figure 40 represents corresponding performance for two successive shift commands spaced 0.7 microsecond apart.

The tests whereby these oscillograms were obtained were made on an eleven stage version of the shifting register, constructed in the form represented by Figures 41 and 42. This unit is now undergoing an extensive life and reliability test expected to continue for about a thousand hours, the test consisting of applying groups of eleven shift commands at megacycle frequency, and having an interval between shift groups of about a millisecond. This scheme shifts any desired pattern of data completely around the register, restoring it to original position during the millisecond wait between shift groups. Hence a stationary pattern is produced in the register indicator tubes, and this



i^{th} Stage of 11 Stage

Conditional Clear Type Shifting Register

Fig. 38

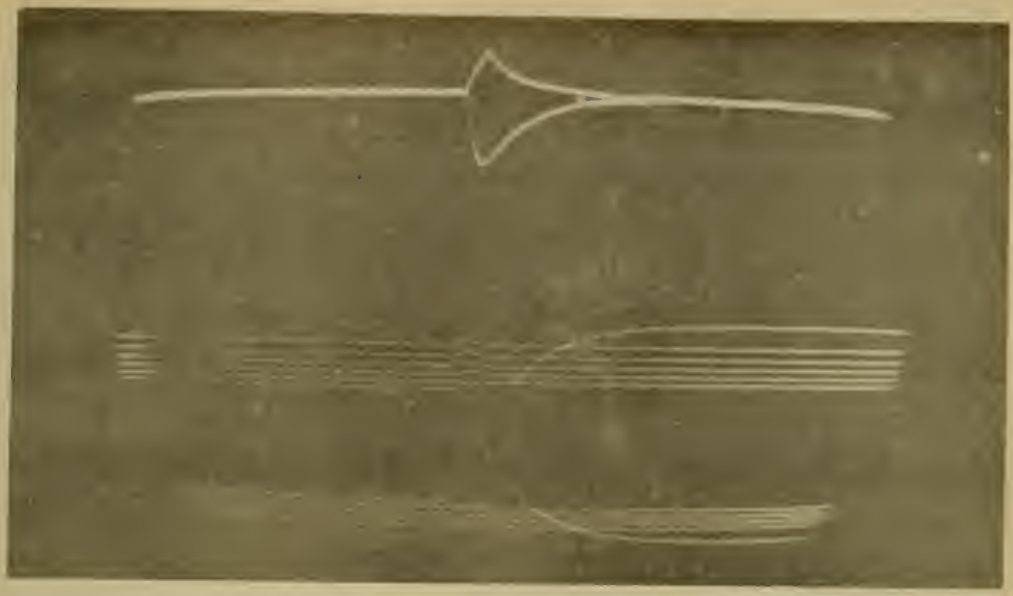


Figure 39

Shifting Register Performance
Top: Pair of activating pulses (Shift and Clear) superimposed.
Bottom: Reaction time of shift for zero and Unity.

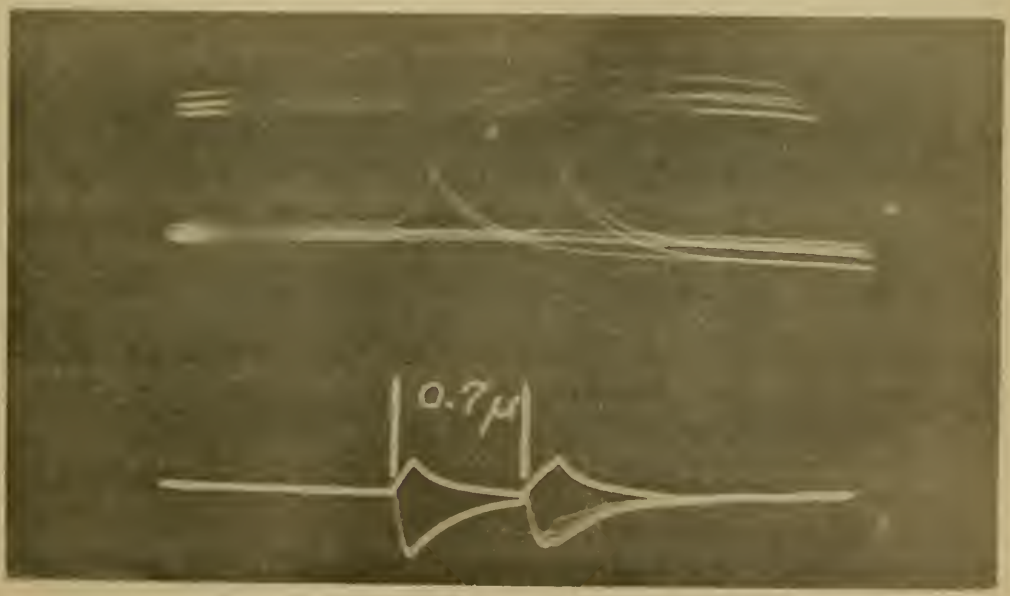


Figure 40
Shifting Register Performance
Top: Reaction time of receiving toggle circuit to shift.
Bottom: Pair of shift activating pulses superimposed.

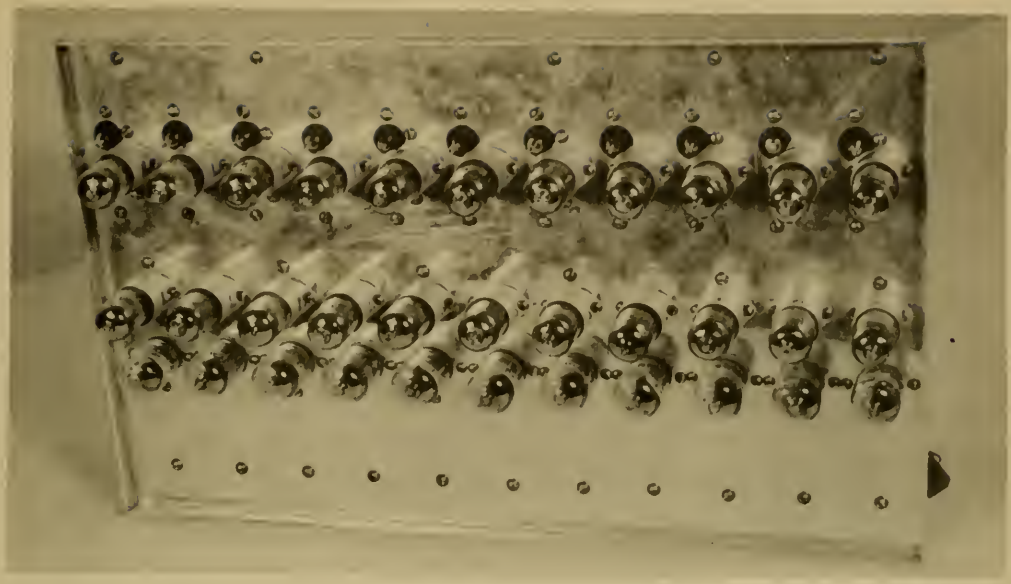


Figure 41
Modified Clear Type Shifting Register

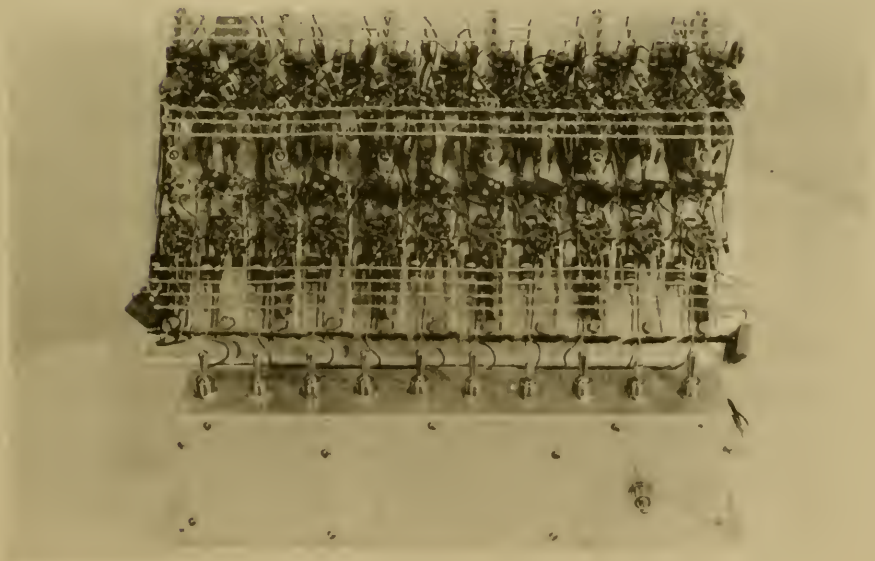


Figure 42
Modified Clear Type Shifting Register

may be tested at will to determine that it does not represent no shifting by changing the shift pulse group to 10 or 12, in which case the pattern becomes blurred.

(2) Shifting Register of Positive Interlock Type.

In Section 10 of P.R. 1 a type of register was discussed which featured the shifting of data from one time-stable binary register cell to the next via an intermediary cell of the same sort, in such a way that the data is at all times held "locked" within at least one of the participating cells. This scheme was contrasted with "delay" shifting schemes in which reliance is placed upon transient storage in RLC networks during the shift. No attempt will be made here to assess the relative merits of the two schemes, but merely to give an account of some of the developments.

The "locked transfer" scheme requires that a "standby" register toggle be available (and vacant) between proper register elements, and that when a shift is commanded, each proper toggle element be connected so as to share its datum with the intermediary; then when the intermediary has received and "locked" upon this datum the donating stage is disconnected and the intermediary is connected to the next proper stage so that the datum is shared, etc.

Clearly this operation could be effected with a high degree of reliability and at a relatively satisfactory speed, if all functions of storage and gating were carried out by "brute-force", that is, by liberal use of tubes. In particular, for a single "stage" of such a register, four triodes could be used; two for the "proper" and two for the "intermediary" toggle cell; in addition, two triode gates could be used to go from the "proper" cell to the intermediary, and two more to go from the intermediary to the next "proper" cell (destination). These gates, in the most naive system (see diagram 43A)

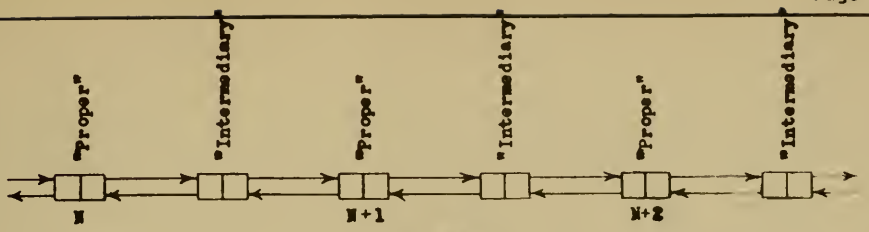


Fig. 43A

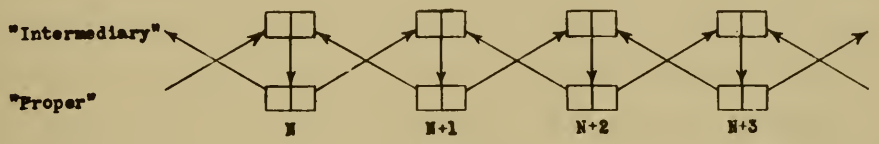


Fig. 43B

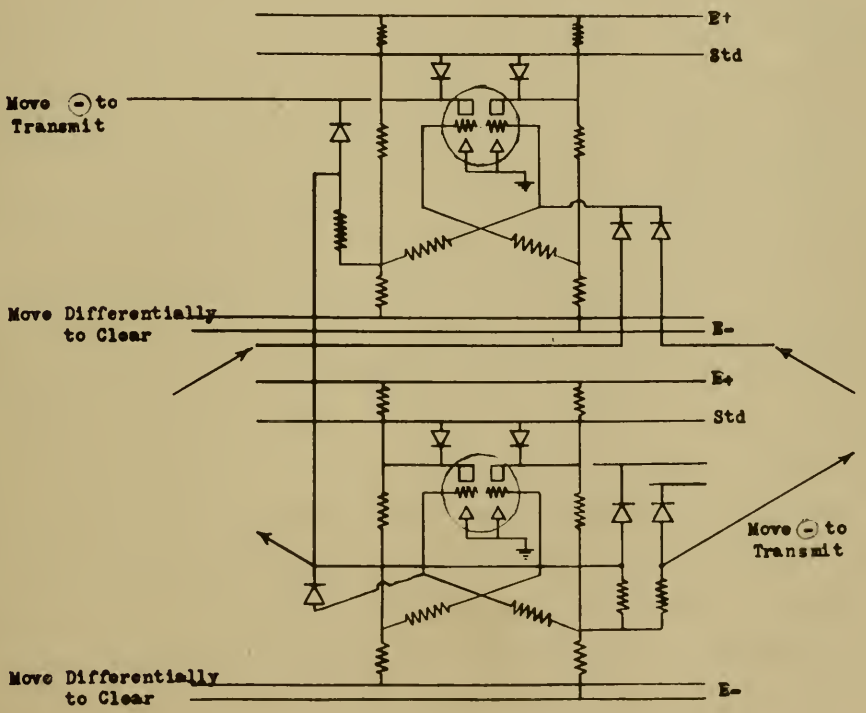


Fig. 43C

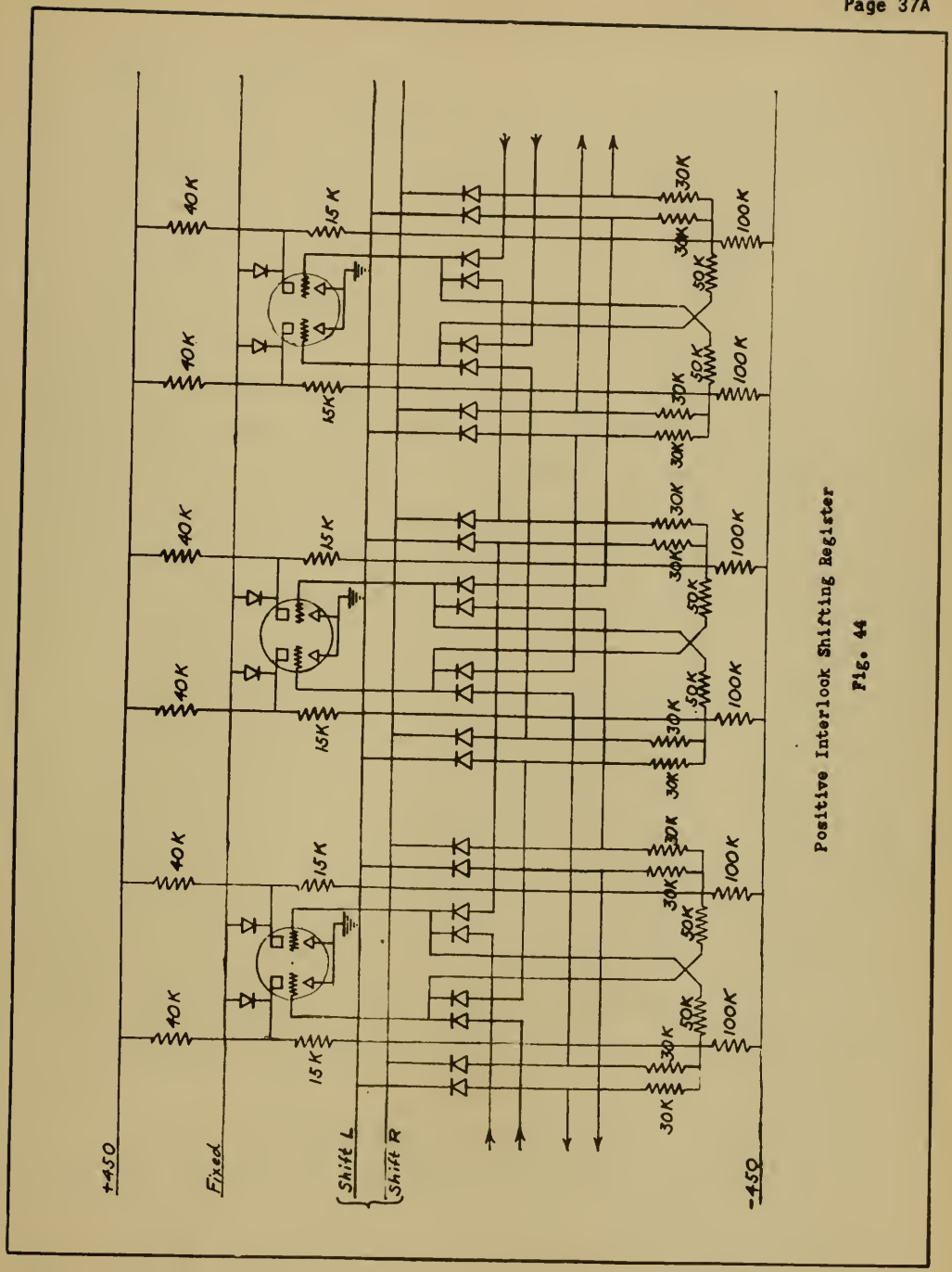
would be duplicated to provide for shift in the opposite direction, so that the total number of triodes per stage would be 12; presumably in six tube-envelopes. This seems quite extravagant according to our present thinking, but the arrangement might prove to have merits other than reliability to justify the extravagance; for example, it is actually capable of storing twice as much data as the usual register when not called upon to shift; also gating possibilities for transfer into and out from the component have more variants, such as complementing, etc. These aspects will be discussed more thoroughly in a subsequent report.

An arrangement eliminating the need for two of the gate tubes in each stage is indicated in Figure 43B. Here the transfer between the "proper" toggle cell and its intermediary is unilateral; the "proper" cell always receiving from its associated intermediary, and always transmitting to the intermediaries associated with neighboring "proper" cell. This arrangement should have the same high reliability as the symmetrical arrangement of 43A; and at the same time requires only ten triodes or five tubes per stage. This may be considered a fair competitor with the "clear" type register discussed earlier in this report, which requires six triodes (or three tubes) plus "delay"elements for each stage.

If the number of tubes per register stage is considered literally as the critique by which a register design is to be judged, recourse may be had to any of a vast number of tricks for making fewer tubes accomplish more functions (usually accompanied by some sacrifice in reliability). Such tricks are equally applicable to positive-locked shifting schemes as to transient-actuated shifting schemes; and there are so many possibilities that the process

of cataloging, analyzing and experimentally assessing their merits is far from complete. For example, one of the commonest schemes involves tricks to be carried out with the means by which a shift is commanded; obviously if the shift command bus be split into two or more arteries and operated separately according to some time schedule, the need for certain gates can be obviated. In fact, such a scheme as this relegates to the shift control component a part of the gating function. Quite similarly special "clear" busses may be provided which make necessary the shifting only of the unity data in a register, rather than both units and zeros; and this will further reduce the gating requirements.

A shifting register circuit of the "positive locked transfer" type represented by diagram A of Figure 43 was designed, built and tested complete in five stages. As indicated in the circuit diagram of Figure 44, crystal gates were used without attempt to economize, there being ten per toggle stage. This circuit was tested experimentally and found to operate well at shift repetition rates of a megacycle and is probably capable of even higher operating rates. As an example of the economies of gating made possible by using special program busses for shifting and clearing and taking advantage of the simplified scheme (Figure 43B) a simplified equivalent to the circuit of Figure 44 is indicated in Figure 43C. It is expected to continue analytical and experimental studies of register components along these lines, but since the several satisfactory types described have been completed, this project is of less urgency than developments pertaining to accumulators, memory and control.



Positive Interlock Shifting Register

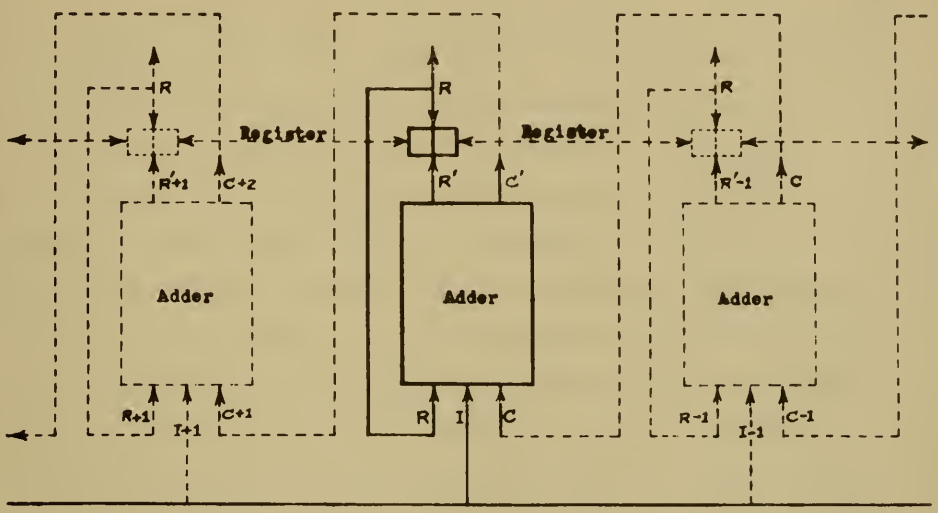
Fig. 44

XI. ACCUMULATOR COMPONENT STUDIES

The accumulator component of the arithmetic organ carries out two essential functions: (1) it provides statically stable storage for a 40 binary digit word, having the ability to shift left or right and to transfer out or receive in parallel, and (2) it contains 40 parallel contrivances, each equipped to sum the binary digits presented at three independent input channels and to produce a signal corresponding to their sum in such a way that each of the two figures of that sum appears on a separate output channel. (See Figure 45A.) The apparatus providing the shiftable storage (1) may be called the accumulator register, while the summing means (2) is called the Adder. Since shifting registers have already been discussed (Section 10) their function is here of interest only in conjunction with the process of addition, and accordingly the adder is the first topic to be explored.

The three binary inputs to the adder may conveniently be called the resident digit (R), the incident digit (I) and the carry-over digit (C). As indicated in Figure 44, these are presented at three separate input channels (R, I, C) and originate at the accumulator register (R), the arithmetic register (I) and the carry (C) of the previous stage. The output consists of two separate channels; one of them (R') offering the new resident digit (which is the right-hand binary figure of the sum) to the accumulator register, and the other channel (C) conveying the carry digit (left hand binary digit of the sum) to the next left adder stage.

Various means for effecting this adder function by means of vacuum tubes, rectifiers, etc. may be devised; perhaps the most direct



Adder Schematic

Fig. 45A

Incident	1	1	1	0	0	0	1	0
Carry	1	1	0	0	0	1	0	1
Resident	1	0	0	0	1	0	1	1

Sum = 000 001 011 111

Sum = {<2, >2} {Even, Odd}

Must Identify: → 1 2 3 4 5 6 7 8 → 1 2 3 4 → 1 2

A. Direct Inputs B. First Kirchoff Sum C. Second Kirchoff Sum

The Adder Problem

Fig. 45B

and certain being to use enough tubes to act as switches or gates, arranged to be "on" for various combinations of digits presented at the three inputs, and deriving the two output signals by switching as the case may require through combination of these gates. This procedure has many merits and is currently being studied; however, most of the schemes thus far developed along these lines appear excessively extravagent in gate element requirements, and to date have not been constructed.

A second approach to the adder problem involves using Kirchoff's laws in some manner such that by summing a combination of three voltages or currents upon a single resistor network, four levels are achieved identifying the four possible sums (see Figure 45B). It is then possible to distinguish the four situations and to actuate the two outputs accordingly by means of gates arranged to distinguish whether the sum is greater or less than two, and whether the sum is even or odd. Alternatively these distinctions can be facilitated by means of a second Kirchoff's law network arranged to subtract twice the results of the first distinction (carry operation: sum greater or less than two) from the sum, then judging by a gate operating on this difference whether the sum is odd or even and so producing the second (R' output) operation. It should be observed that while the use of Kirchoff's laws twice in succession appears to reduce the number of situations to be identified by gates from eight to two (Figure 45B) the advantages are in reality by no means so great, for in using Kirchoff addition with linear (resistive) circuit elements and applying the rules of ordinary rather than binary algebra, it becomes necessary to quantize the input data, which requires tubes (gates) to substitute scalar entities for binary data. The question of whether or not it pays to use Kirchoff summation

thus boils down to a question of whether the conversion from three binary to three scalar quantities (which is necessary if these quantities are to be added to and subtracted from each other in ordinary algebra), and the subsequent conversion of the results back into two binary quantities may more readily be carried out with the circuit elements at our disposal than the strictly gating operations in which binary inputs are never added to or subtracted from each other but merely compared each to a standard reference (decision) point in order to determine sign.

A Kirchoff summation type adder was developed in experimental form and constructed in ten stages, primarily for the purpose of studying propagation rate of carry signal; the importance and various aspects of this problem are discussed in L. D. 1, Sections 5.5-5.6. The outfit is shown in Figures 46A and B, and the circuit diagram indicated in Figure 47. This binary adder operates as follows: A double triode toggle circuit consisting of a 6J6 tube cross-connected in conventional fashion stores each of the inputs R and I statically. Leading out of one of the plates of each of these toggles is a summing resistor (220 K ohms) which are joined at a summing bus that is also acted upon by the carry input. Since each of the toggles R and I swings at its plate between fixed voltage limits, the summing resistors each contribute a unit of voltage swing to the summing bus. The carry input from the preceeding stage also swings the voltage summing bus via a 180K resistor to contribute the third addend to the voltage sum. The voltage swing of the carry input lead is bracketed between crystal rectifiers rather than standardized by a toggle plate swing, as will be reexamined in what follows.

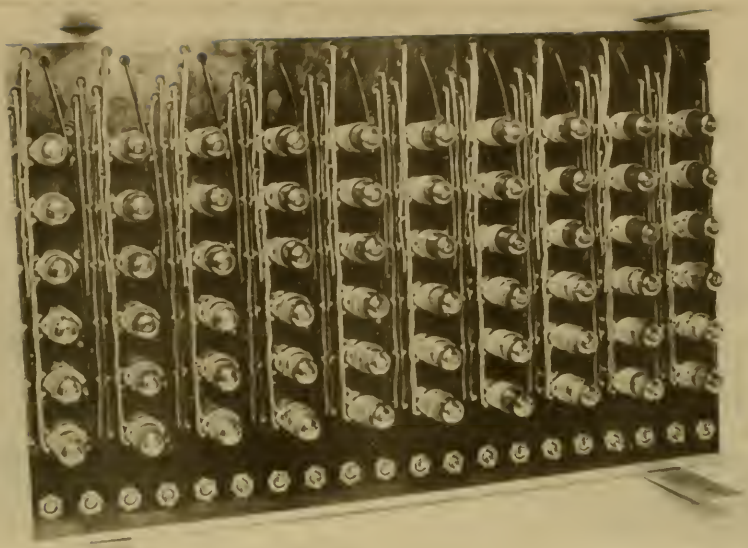


Figure 46A
Adder

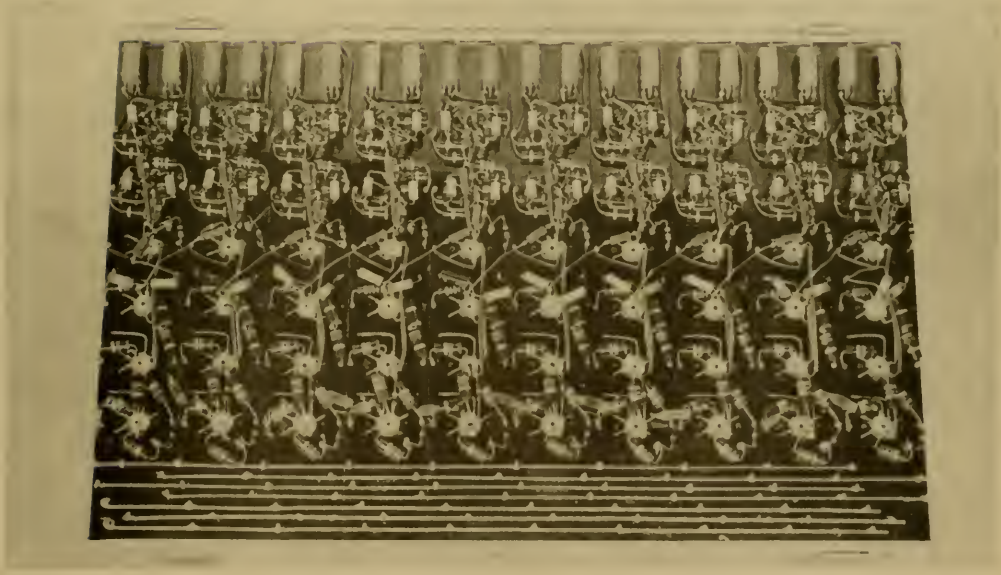
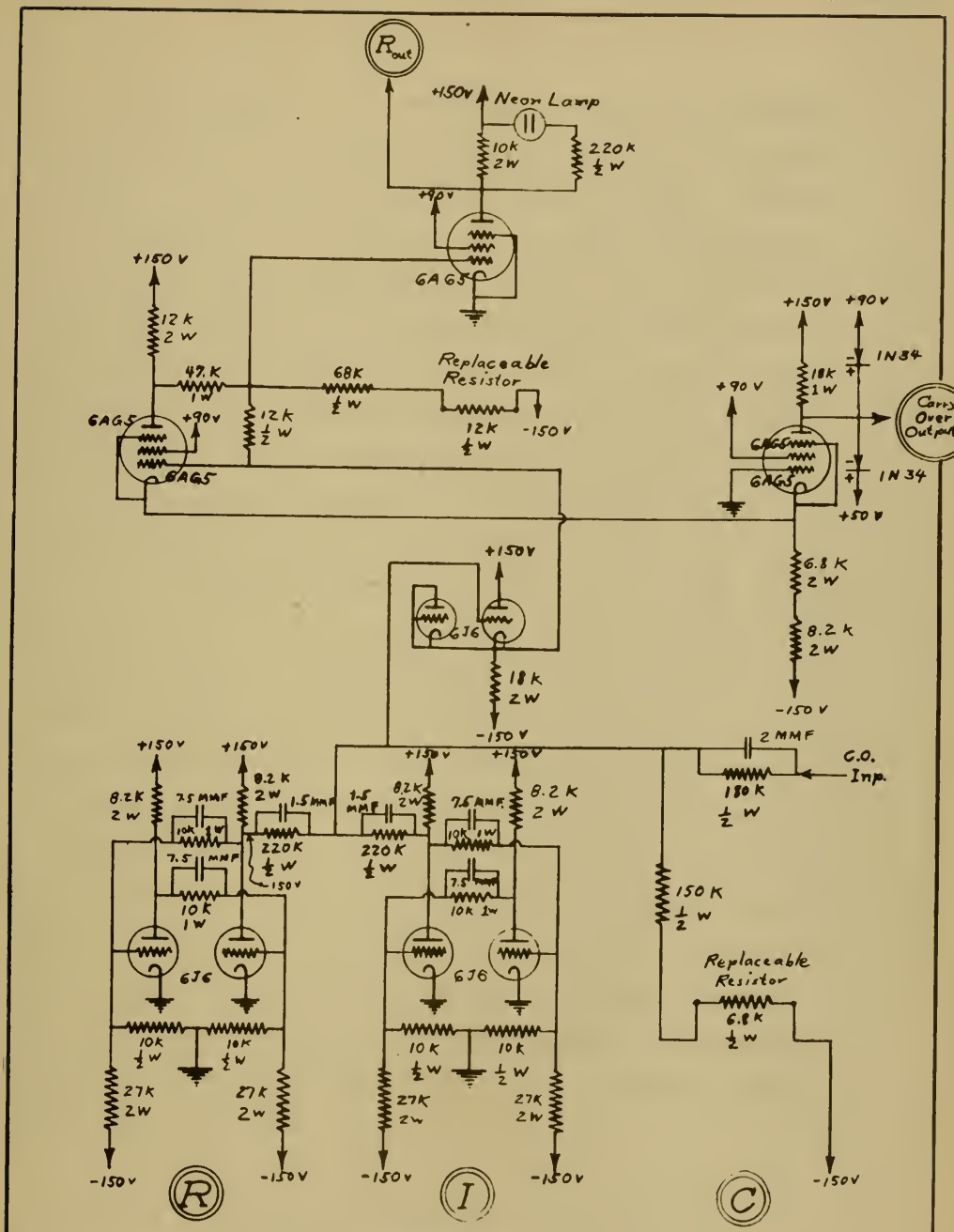


Figure 46B
Adder



Binary Adder

Fig. 47

The voltage on the sum bus is placed on the grid of a cathode follower (D) and so is reproduced at higher current level; this is then placed on the grid of a 6AG5 sharp cut-off pentode (B) which is cathode-follower coupled to a second 6AG5 pentode (C). These two tubes, plus a second Kirchoff summation network (12, 47, and 68 + 12K) are intended to carry out the operations of distinguishing whether the sum be greater or less than two, and whether even or odd , as follows: For the case when all inputs are zero the voltage from the sum bus reaching the grid of tube "B" keeps it cut off, so no current flows in the plate, which is positive and contributes accordingly via the 47K network resistor; however the effect of this on the second sum voltage value is over-ridden by the negative contribution via the 12K network resistor arriving directly from the first voltage sum bus. Accordingly the sum point and hence the grid of resident digit output amplifier tube "A" is cut off and so "no digit" is indicated. Likewise no current being drawn through the cathode coupling link between B and C, the cathode of C is held positive by its own grid and hence the plate of tube C is negative, signalling "no carry" at C + 1. Next, in case of a single unit and two zero inputs are presented to the adder, the first voltage sum bus goes one unit positive, which is not sufficient to affect tube B and hence does not effect tube C; however the positive swing arriving directly on the second summing point via the 12K resistor swings the second summing point and hence the grid of tube A positive, signalling a unit output for the new resident digit.

In the event of two unit inputs and one zero being presented (at R, I, C) to the adder, the grid of tube B is now forced positive and so the plate comes negative, extinguishing the resident digit output amplifier by overriding the second summation with negative voltage. Also when tube B draws current, the cathode of tube C is hauled positive, extinguishing the tube and allowing the plate to swing positive and signal a carry.

In the event of all three adder inputs being positive, tube B continues to be on and tube C, being off, continues to signal carry; however, the third positive voltage increment arriving directly at the second voltage sum point via this 12K network resistor from the first voltage sum bus has the effect of overpowering the second voltage sum, making it positive, signalling a new resident digit via amplifier A.

This circuit, when properly set up, carefully adjusted and padded at the resistor networks with suitable accelerating condensers as shown, was found able to propagate a complete carry through ten stages in about one-half microsecond. This experiment implied about two microseconds carry time for 40 stages as being quite realizable, and so justified continuation of the type of development. Aside from illustrating achievable speeds of carry propagation, the circuit was (as might readily have been predicted) highly capricious and unreliable, and required careful adjustment each time prior to any operating tests. In particular, the two standard toggle circuits storing "R" and "I" are by no means adequate to quantize these accurately enough to be added algebraically to form four voltage levels; furthermore, the method of quantizing the addends in the second Kirchoff summation depends directly

upon the sum values in the first summation; and the subtraction of two units from the sum in the event of a carry is accomplished through an amplification system (tube B) referring to the original sum voltage rather than to a new and reliable reference point.

A succession of adder circuits were developed and investigated experimentally; these included use of crystal rectifiers to bracket voltage swings of all three addends, as done in the circuit of Figure 47 for carry digit only; also the use of specially designed toggles such as cathode-coupled toggles with high degeneration, and of various combinations of current and voltage summation in circuits having special attention devoted to achieving constant current or constant voltage increments. This development program is still in full swing, and it does not appear worthwhile to present a detailed discussion of all the evolutionary aspects at this time.

A complete accumulator circuit recently developed, consisting of a double-Kirchoff current and voltage adder plus register storage and transfer gates is shown in Figure 49 as built in eleven stages. The circuit diagram of this accumulator is represented in Figure 48, and since the arrangement shows some promise of eventually reaching a fair state of reliability and has a carry propagation of about .6 microseconds for eleven stages, it may merit brief discussion. Starting from the left, a pair of 6J6 twin triodes are arranged in a highly degenerative cathode-coupled arrangement so as to provide zero current or a constant current of 8 milliamperes to the current summing point (directly above the carry input). These triodes are so cathode-coupled as to allow complementing the incident digit from the register for subtraction.

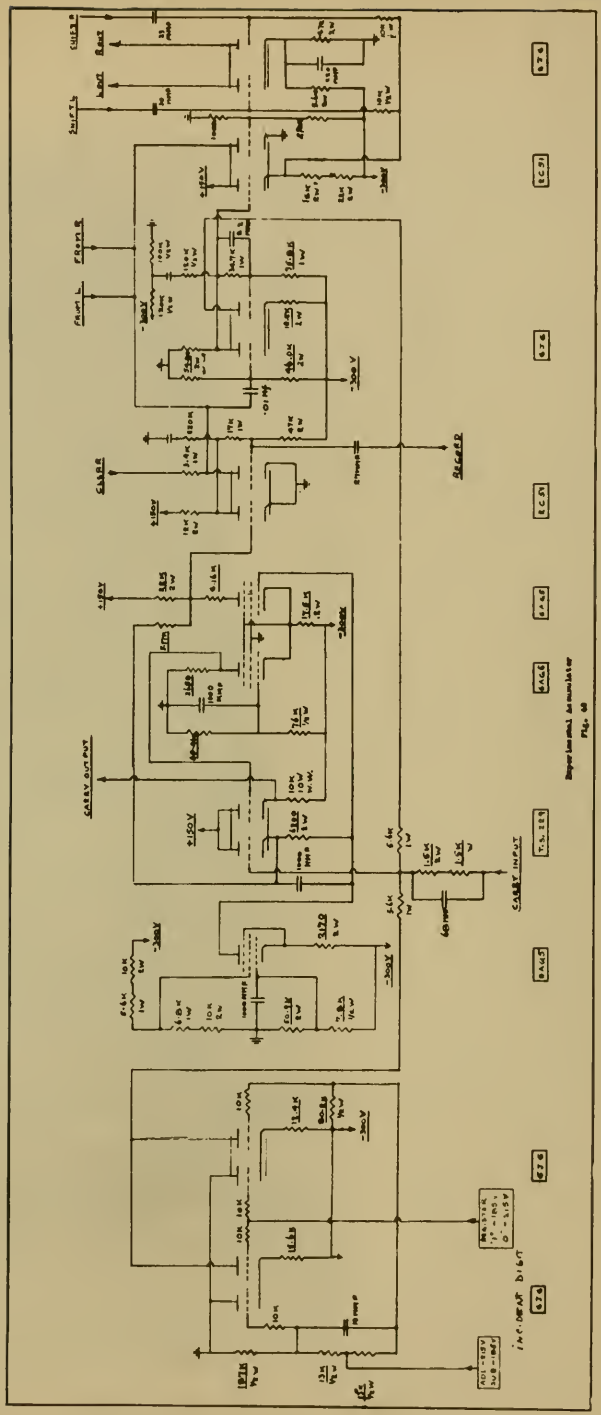


Figure 49
Eleven Stage Binary Accumulator,
Experimental Kirchoff Summation Type

Also entering the first summation point is the carry input from the previous stage, which instead of being a unit of current is a fixed voltage step determined by a substantial cathode follower system (229 tubes). The third addend is a current coming from the right, and comprises the resident digit in the accumulator. The result of this summation of two currents and one voltage appears as a voltage across the 3K standard resistor and appears at the cathode follower grid (229) directly above. Duplicated and strengthened, the sum value proceeds to a second Kirchoff summation network which , in conjunction with two 6AG5 tubes, operates so as to produce carry output and resident digit output signals quite like that just described in the previous adder.

The resident digit output (R') is next amplified and gated by means of a pair of 5C51 triodes, permitting the accumulator register stage (Next right; 6J6) to be cleared and to have recorded upon it the new resident digit R'. The accumulator register stage receiving R' is a cathode-coupled toggle and contributes via its right plate lead one of the standard 8 mill currents to the first summation, as mentioned above. In conjunction with this there are arranged a set of gates ordering the register to shift right, left or to transfer in or out.

Studies of this arrangement are not yet complete, but some satisfactory tests as to speed and potential operability have been carried out, and are encouraging. Already numerous improvements have been proposed and are being investigated by analysis and experiment.

XII. CONTROL COMPONENT STUDIES

The problem of evolving an adequate control organ for the computing machine has two aspects (1) the logic of planning programs of operations appropriate to the control theory, and (2) the technical problem of realizing the individual operations demanded. These two aspects must be considered jointly at all times in order that the best compromises be reached.

One of the most obvious and immediately required components for the control organ takes the form of a sort of "pulser", capable of producing at its output a high energy pulse suitable for operation of ganged-element busses located in the arithmetic organ. This pulser should produce a high-energy pulse on the bus each time its input is so commanded, and it should be capable of operating at megacycle repetition rates. The preferred form of output pulse is roughly rectangular or "flat-topped" rather than peaked, and the duration half a microsecond or less, of perhaps 100 volts amplitude in the presence of several hundred mmf load capacitance.

This list of requirements is not at all easy to meet, and in fact, if the requirement of a high duty cycle is added, the problem becomes a formidable assignment.

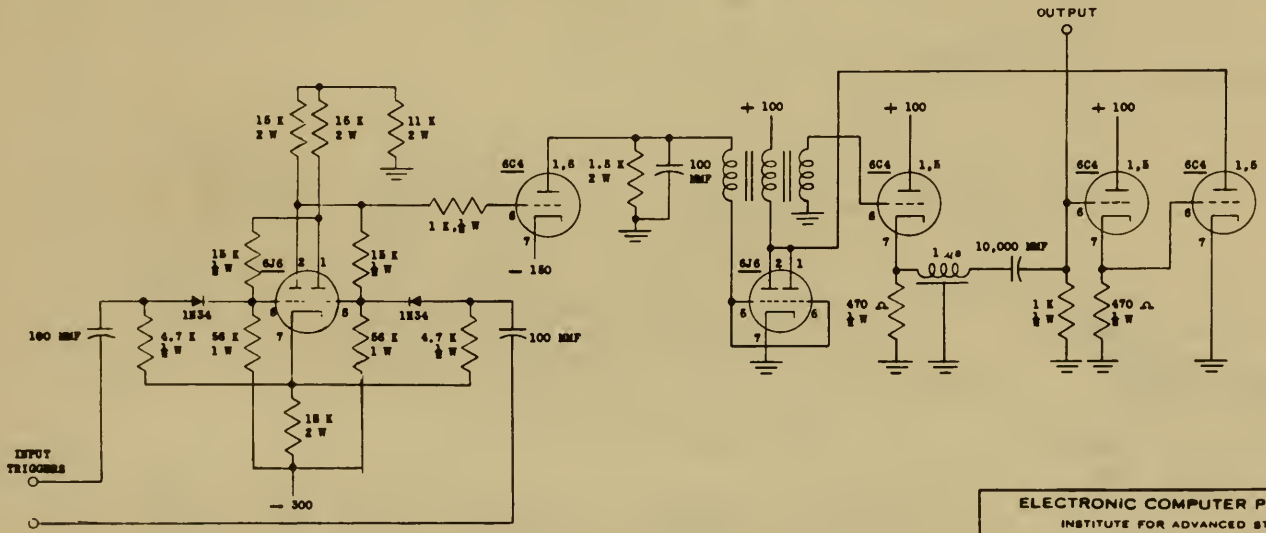
An attack has been made along the lines of developing and extending the performance of the usual variety of blocking oscillators. These normally produce suitable high energy pulses, but have a self-running frequency on the order of a few hundred kilocycles; a limit apparently set by the transformer recovery-time. If a sufficiently violent trip-off pulse be introduced after an interval shorter than that of the free-running relaxation-recovery, the oscillator can be

hastened, and a pulse repetition rate of one megacycle having .4 microsecond width in the presence of 500 uuf load capacitance was attained in this way. The arrangement is indicated in diagram C-3-1008 and may be seen to include two stages of current amplification, a trigger tube and a delay line for timing the accelerating pulse. A useful accessory feature was included making it possible to "gate on" or "gate off" the oscillator after a predetermined string of pulses have elapsed. Further development of blocking oscillators is in progress.

A second example of pulse generator of this type is represented by diagram C-2-1017, and was constructed in the form shown by Figure 27. This device is capable of issuing a single high-energy pulse each time commanded, at a maximum repetition rate of 1.5 megacycles, and maximum duty cycle of about 30%. The output pulse is flat-topped and controllable in width from .2 to 2.3 microseconds (see Figure 28), has a rise and fall time of about .1 microsecond, and is controllable in amplitude from zero to about 80 volts. The source impedance is about 200 ohms.

With the completion of a satisfactory shifting register component (Section 10) and the completion of the first potentially satisfactory accumulator component (Section 11) it becomes expedient to begin synthesizing the first elementary sections of the control from gates and pulser components of the type described above. Figure 49 represents a primitive attempt in the direction of controlling the shifting register and accumulator components of the arithmetic organ so as to effect multiplication of positive binary numbers.

The process of multiplying binary numbers consists of (1) clearing the shifting register and accumulator register by placing a start pulse at

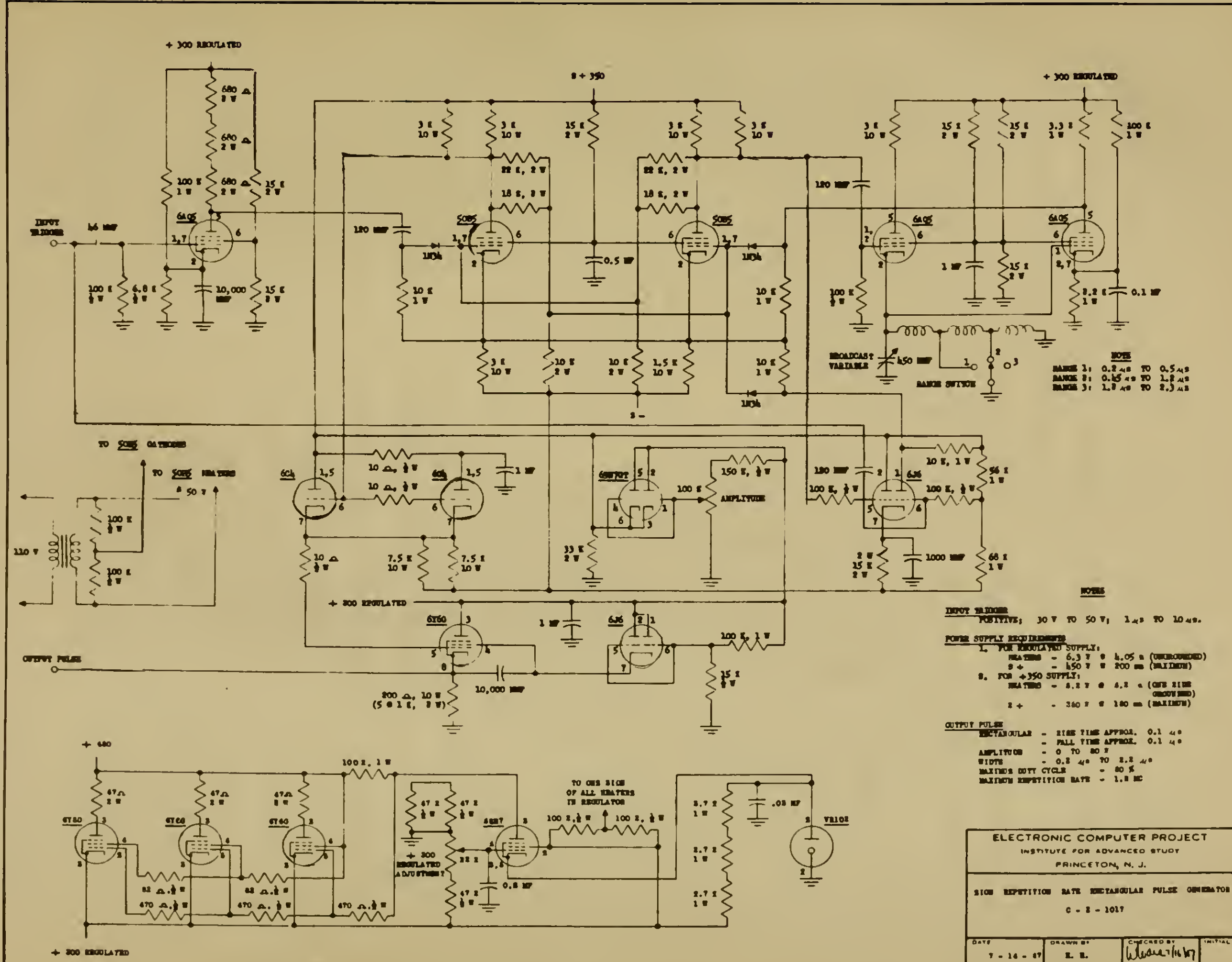


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.

ONE - MEGACYCLE PULSE GENERATOR

C - E - 1008

DATE	DRAWN BY	CHECKED BY	INITIAL
7 - 14 - 47	E.E.	7/16/47	


ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.
HIGH REPETITION RATE RECTANGULAR PULSE GENERATOR
C - 2 - 1017
DATE 7 - 14 - 47
DRAWN BY R. R.
NOTES
INPUT TRIGGER
POSITIVE; 30 V TO 50 V; 1 μs TO 10 μs.
POWER SUPPLY REQUIREMENTS
1. FOR REGULATED SUPPLY:
HEATERS - 6.3 V @ 4.05 A (UNGROUNDED)
B+ - 450 V @ 200 mA (MAXIMUM)
2. FOR +350 SUPPLY:
OUTPUT PULSE
RECTANGULAR - RISE TIME APPROX. 0.1 μs
- FALL TIME APPROX. 0.1 μs
AMPLITUDE - 0 TO 80 V
NOTE
INPUT TRIGGER
OUTPUT PULSE
+ 300 REGULATED
B + 350
RANGE SWITCH
BROADCAST VARIABLE
AMPLITUDE
TO ONE SIDE OF ALL HEATERS IN REGULATOR
110 V

A2 of Figure ; this pulse passes via 27, 17, 5/6 to emerge at A10, (accumulator clear) and also via 27, 17, 9/10 emerging at A8 (register clear). (2) Since the digits in the multiplier must be counted in order to terminate the process at the 40th cycle, there must exist a counter (32, 45, 32, 46, 33, 47, 33, 48) which must be cleared prior to multiplying by the first digit in the shifting registers. This clearing is also accomplished by the initiating pulse of step (1) via 27, 17, and 30. (3) Next, transfer the multiplier into the shifting register; this is accomplished by the same initiating pulse as step (1) delayed, however, by .05 microsecond before passing through 28, 18, 7/8 to emerge at A12 (register receive multiplier). (4) The initiative is now assumed by input C(0/1) which inspects the first digit of the multiplier, sending the information through gate 24 whence, if a zero, it follows the upper track (38, 37, 31, 23, 15) to emerge at accumulator clear A10 and also passes to the counter (via 29, 34, 42) after a microsecond delay, and also to the "OK next digit gates" (25 and 38) via 41. Also the pulse passes after .05 microsecond delay via 36, 22, and 13/14 to emerge at A6 "Shift both accumulator and register right". In case of a unit instead of a zero at C(0/1) the lower channel is followed after 24; namely (25, 40, 26, 16) producing the accumulator clear pulse at A10 exactly as in the case of a zero; and likewise actuating the count and accumulator and register shift. Via 39, a one microsecond delay and 44, the unit signal also proceeds to 35, 21, 11/12 and emerges at A4 commanding the accumulator to record the new sum in its register. The cycle may then be reinitiated by C(0/1) when the gates 38 and 25 indicate completion.

A circuit intended to carry out these control functions has been evolved and is presented in very nascent form in Figure 50. The construction of this circuit has just been completed and is at present undergoing experimental assembly and trouble-shooting. The construction is shown in Figure 51.

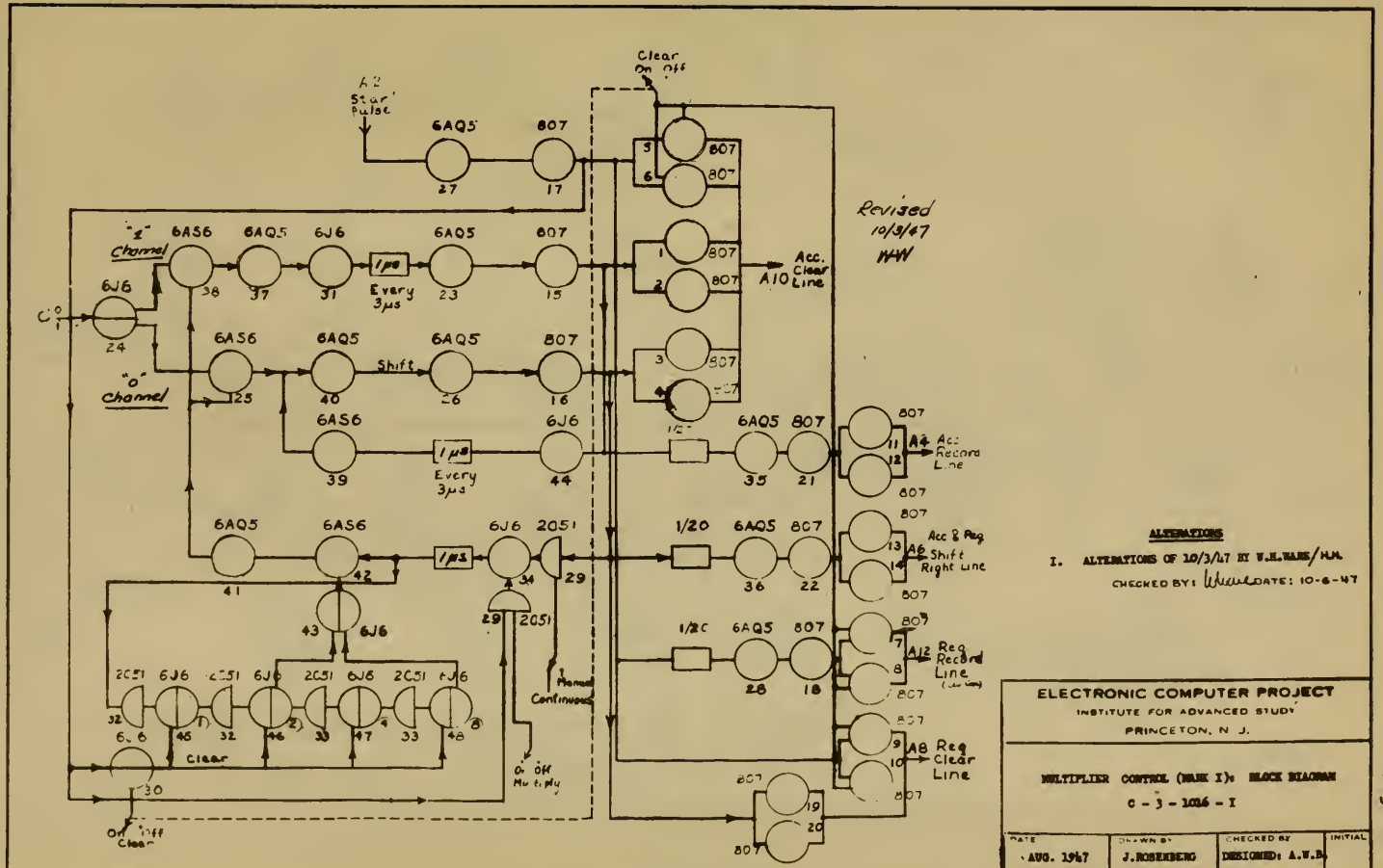


Figure 50

Schematic of Experimental Multiplier Control

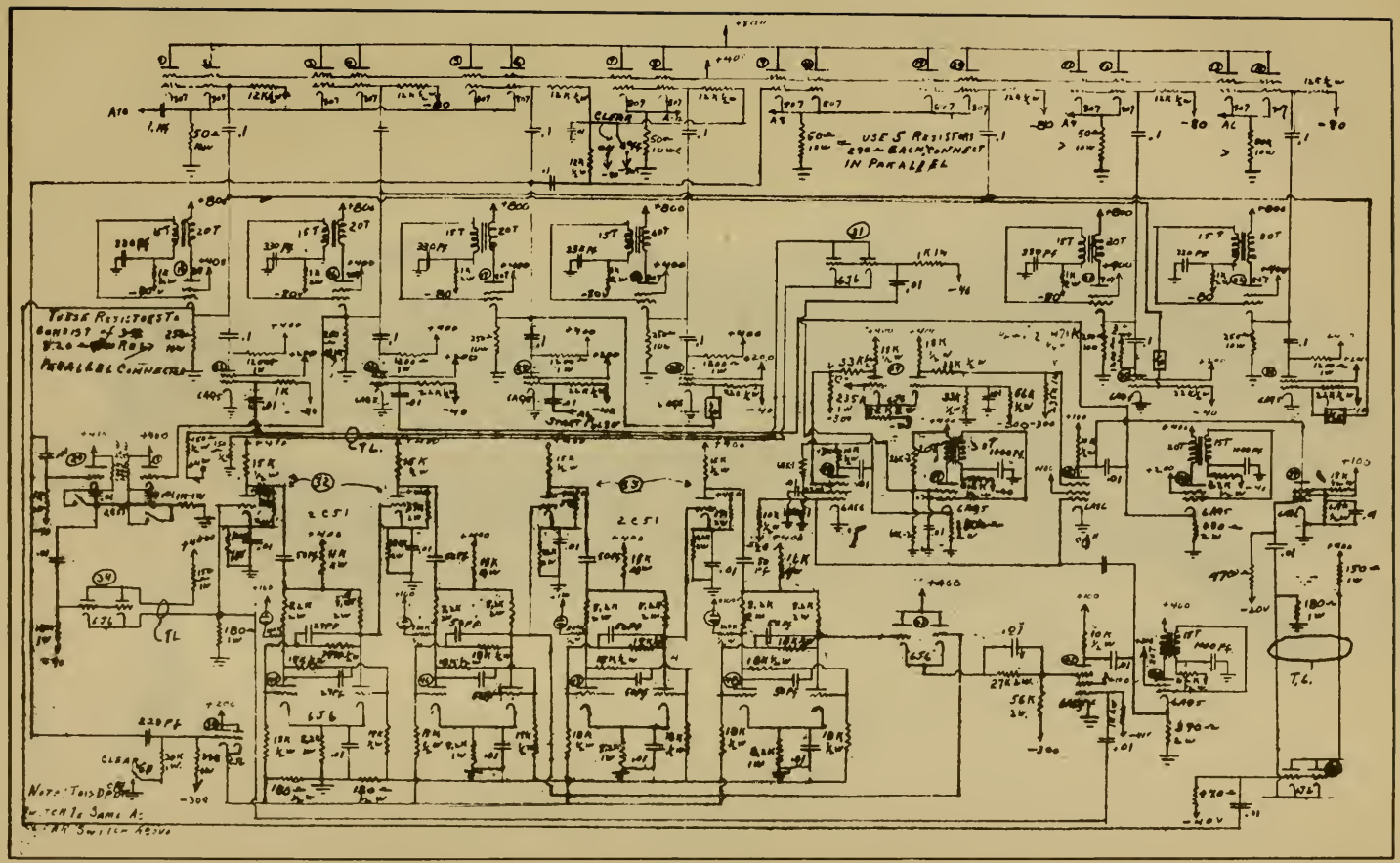


Figure 51

Multiplier Control Circuit, Experimental

Figure 52
Multiplier Control Chassis, Experimental