FINAL REPORT

on

CONTRACT No. DA-36-034-ORD-1646

PART I (ENGINEERING)

by

The Staff
Electronic Computer Project

THE INSTITUTE FOR ADVANCED STUDY
ELECTRONIC COMPUTER PROJECT
PRINCETON, NEW JERSEY

FINAL REPORT

on

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PART I (ENGINEERING)

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The following report has been prepared in accordance with the terms of Contract No DA-36-034-ORD-1646 and constitutes the Final Report called for under the terms of that contract.

Said Contract between the Institute for Advanced Study and the Department of the Army was entered on June 2, 1954, for "further development of principals and methods for operation and maintenance of very high speed digital electric computer devices", i.e. for continuation of our work under Contract No DA-36-034-ORD-1330, which terminated on June 30, 1954, and for which a final report was submitted, dated December 1954.

Contract No DA-36-034-ORD-1646, together with its supplemental agreements No.1 and No.2, was in effect from July 1, 1954 through October 31, 1956, and was the only contract supporting maintenance and operation of our Computer during that period, except for the last 7 months during which a small part of the operation has been paid for under Contract Nonr-1358-(04). This new contract between the Institute for Advanced Study and the Office of Naval Research has taken over the full burden of machine maintenance and operation on January 1, 1957.

This Final Report is divided into two parts:

PART I covers the engineering work carried out from July 1, 1954 through December 31, 1956 under the terms of Contract No. DA-36-034-ORD-1646.

PART II lists a number of problems for which, during the same 30 months, numerical results have been obtained with the help of our Computer. This work was supported by four contracts:

(1) Contract DA-36-034-ORD-1646 and Nonr 1358-(04) for machine operation.

(2) Contract N7-onr-388 for the development of methods for high-speed automatic computing (from July 1, 1954 through December 31, 1954).

(3) Contract Nonr-1358-(03) for the development of methods for high-speed automatic computing (since January 1, 1955).

(4) Contract Nonr-1358-(02) for all mathematical and coding work connected with meteorological research.

During the whole period our Computer was used for scientific computations exclusively and no charge was made to any other organization or contract for coding or machine operation.

51706

Hans J. Maehly
Acting Project Director

INTRODUCTION

This report describes the operation of and engineering improvements on the electronic computer at the Institute for Advanced Study during the period from 1 July 1954 through 31 December 1956. A full technical description of the machine prior to this period is given in the final reports on Contract No. W-36-034-ORD-7481, Contract No. DA-36-034-ORD-19 (Project No. TB3-0007F), Contract No. DA-36-034-ORD-19 (Project No. TB3-0007), and Contract No. DA-36-034-ORD-1330 (Project No. TB3-0538).

ACKNOWLEDGMENTS

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A. ENGINEERING WORK

1. New External Control and Drum System.

a. Introduction.

Early in 1955 the need for additional memory capacity in the computer had grown sufficiently acute to justify an active program in this direction. The machine at that time had essentially three levels of memory: 1024 words of high speed electrostatic (Williams) storage, 2048 words of medium speed magnetic drum storage, and arbitrary amounts of punched card storage. A large increase in high speed storage would have been useful but the resources of the project limited consideration to the medium speed level. Accordingly plans were begun for adding a new magnetic drum of at least 10,000 words capacity. A suitable unit was found in the ERA type 1107 magnetic drum which would provide for up to 16,384 words stored on a return-to-zero basis.

Because the new drum was to store 8 times as many words as the existing one and because the block transfer restriction and relay switching of the old drum had proved unduly burdensome and time consuming it was decided to design and construct completely new circuitry for the new drum. This decision opened the way for a careful re-examination of the logical relation between the central computer and its input-output gear.

The IAS computer was originally provided with a modified Teletype system which was connected in by manual switching whenever loading or unloading was desired. This slow and cumbersome arrangement was soon replaced by a punched card system whose operation was commanded automatically by explicit machine orders. Aside from its speed limitations

the punched card system has been very satisfactory but it is quite in-
flexible with respect to additions of other input-output equipment.

The existing system is logically unsatisfactory in that each
kind of input-output operation is given a separate order in the basic
machine list and thus accorded the same status as the arithmetic opera-
tions. However, the arithmetic orders are completely specified by one
memory address and one operation command, whereas the input-output
orders must specify not only one memory address (i.e. the starting point
of the reference in the high speed memory) but also at least one other
address (i.e. the starting point in the input-output unit) as well as
another address-like quantity which is the number of words to be trans-
ferred. Again, the input-output orders, though numerous as to variety,
occur very much less frequently than arithmetic orders in the average
code and are usually relatively slow.

Since input-output orders are more complex, occur infrequently,
and are slow one is led to consider them a sub-class of the basic high
speed order list. We extend this notion further. In referring to a
basic high speed order list we really have in mind the core of the high
speed computing system, a fast memory-arithmetic unit-control complex
within which most of the computing activity occurs. External to this
complex are all the input-output paraphenalia: magnetic drums, tapes,
punched cards, graphing oscilloscopes, human beings, etc. Information
flows through these media into the basic complex where it is resolved
into numbers and orders causing operations on the numbers. All opera-
tions, whether internal only, or between internal and external only, or
between external and external, are commanded by orders decoded in the

basic complex. To it all external devices are slaved.

The order list should then be split into two parts. One part comprises the internal operations which are fast and involve typically only one operand. These might be called the basic, or internal orders. One of them is set aside to denote reference to the other part of the order list, the external operations. The external operations are not specified by information in the order register of the basic complex but rather by information transmitted to the external unit and decoded therein. At least two advantages stem from this treatment of orders:

1) The basic order list can be kept small. This is important to both user and designer and has some bearing on speed.

2) Alterations and additions can be made to the external operations independently of the basic complex. This permits the computing system to evolve with the needs of the user.

To gain these advantages some price must be paid. Generally speaking some extra equipment is added because of the duplication of functions. Specifically the following is certainly needed:

1) An external control unit to decode and direct the external orders.

2) A buffering register to present consistent data transmission conditions to the machine (basic complex) and to permit external operations while the machine is doing other things.

Following the above philosophy a new input-output system was

constructed for the IAS machine. Although only the central external control and the local circuitry needed by the new drum was fabricated, the basic design purpose was to provide a system easily adaptable to additional external devices, such as punched card equipment, magnetic or paper tapes, and graphing oscilloscopes. The circuitry is therefore divided both physically and logically into two parts: 1) elements common to any input-output function, and 2) elements peculiar to the drum. The common elements consist of a 40 digit buffering register with parallel connections to and from the machine, a 14 digit counter to determine the specified number of words to be transferred, and the basic external control. The strictly drum elements are the reading amplifiers, writing pulsers, channel switches, angular location counter and coincidence circuit for a specified angular location count.

Most of the information needed for a drum reference will be given by a "priming" word which must be in the quotient register (RII) as the drum reference is begun. This priming word will specify the starting location on the drum (14 digits); the number of words to be transferred (14 digits); the sending unit, which may be the Williams memory, drum, IBM, or perhaps a tape (5 digits); and the receiving unit, which again may be any of the above or a graphing device (5 digits).

Our new machine order will command the actual start of a reference, and its address portion will specify the starting address in the Williams memory. The reference begins with a set-up phase during which the priming word is observed and used. Then the selected sending unit is instructed, subject to its own timing requirements, to transmit its first word into the buffering register. Receipt of this word initiates

the receive half of a word cycle during which the buffering register transmits to the selected receiving unit, again subject to that unit's own timing requirements. This word cycle is repeated until the specified number of words have been transferred after which the order terminates.

A special checking operation is provided for machine to drum transfers. It consists of the actual transfer followed by an immediate repetition in which the previously written information is read back from the drum and compared word for word with the information coming from the machine. The comparison is done in the adder and inequality of any word pair will result in an error indication.

The equipment described on the following pages consists of two major devices. One is a general control for implementing all input-output functions for the computer and providing communication between computer and external equipment. The other is the circuitry which has been provided for the installation of a new magnetic drum auxiliary memory.

The external control device is brought into play by the computer whenever any equipment other than the main computer is required; i.e. magnetic drums, tapes, IBM, graphing, etc. This external control is required to temporarily take over a prescribed controlling routine during any external operation, the computer being subservient to it during this period. Upon completion of the external operations, normal control is restored to the computer and normal operation resumes. Detailed logic and circuitry for this device are described in section b.

Installation of a medium speed auxiliary magnetic drum memory of 16 times the capacity of the main electrostatic memory required develop-

ment of extensive logical and information handling circuitry. Description of this equipment will be found in section c.

A brief description of the physical construction and operating experience to date is given in section d.

b. External control.

i. Overall functions.

The external control remains in a quiescent condition until such time as the computer comes to an order requesting some external function. Prior to the appearance of this order, designated "execution order", a 40-bit "priming word" must have been established in R_2. The function of the priming word is to provide the external control with the starting address in the external unit, the number of 40-bit words to be transferred, and designation of the sending unit and receiving unit. Organization of this word is as follows:

2^0	2^{-15}		2^{-39}	
STARTING ADDRESS	NO. OF WORDS	SENDER	RECEIVER	R_2
14 BITS	14 BITS	5 BITS	5 BITS	
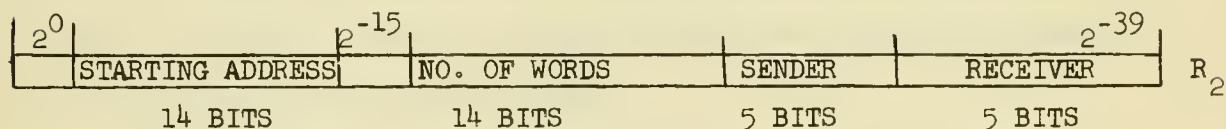
The five-bit group for either sender or receiver is coded as follows:

10000	TAPE UNIT
01000	NEW DRUM
00100	IBM
00010	GRAPHING
00001	WILLIAMS MEMORY

At present only the new drum and Williams memory functions are available;

provision for use of the other facilities has been made.

The execution order, brought into R_3 from the Williams memory contains the Williams memory starting address and a unique combination of order digits in the first phase. The second phase is used to transfer the control, and comes into play at the conclusion of the external operation. This execution order then is as follows:

STARTING WMS. ADD.	1000000000	TRANSFER CONTROL	R_3
1		2	

Word transfer between the computer and external control is accomplished by communication from R^3 to an external buffering register in one direction, and from this register to R_1 in the other direction. These two sets of 40-digit lines together with a small number of logical command signals constitute the entire communication of the computer with the external equipment. All input-output organs will ultimately connect to the computer via the external control.

The following description of this new system will be made with reference to the new magnetic drum.

When the execution order appears in R_3 the following events occur. The Williams order counter is set to the desired starting address and the priming word is transferred from R_2 to R^3. At this time a recognition of the command for an external operation is made by the external control, and the priming word is transferred from R^3 to the external buffering register, ER.

The computer remains in the execution order state until its main

control receives a termination of order signal from the external con-
trol. It is a function of the external control request that a new data
word be brought from or stored in the Williams memory and then finally
to request termination of the entire process.

Upon reception of the priming order by the external register
(hereafter referred to as ER), proper distribution and recognition of
its components must be made. Since the ER will subsequently be used to
transfer numerical information, it is required that the priming order be
used and stored immediately where required for the duration of the ex-
ternal operation.

At "set-up" time then, the four components of the order are trans-
ferred from ER to the proper recognition devices.

Those digits of the priming order which specify the number of
words to be processed are transferred (as inverted digits) to a counter
in the external control device. This "event" counter, known as E.C. is
then used to count with each subsequent word transfer, producing a satis-
faction signal after the required number of words or "events" have been
handled. This unique satisfaction signal is used to initiate termination
of the cycle.

The two five-bit portions of the priming order will each have a
single "one" digit specifying the sender and receiver, respectively. At
set-up time these digits are used to set toggles which then will "re-
member" for the duration of the cycle that portion of the order.

In the case of the drum, the starting address is presented to a
recognition circuit. When the proper drum address has been arrived at,
a process is initiated which will begin information transfer. Since the

drum addresses will remain in step sequentially after starting recogni-
tion, this portion of the priming order will no longer be required.

Thus the earliest possible destruction of the priming word in ER
can occur only after drum recognition of the starting address. (This is
also true for any tape unit, of course, though no starting address is re-
quired for IBM equipment.)

Suppose that it is desired to write on the drum, i.e. transfer in-
formation from the Williams memory to the drum. Conditions which result
from the set-up operation initiate an action request in the Williams
control of the computer. Subsequently the desired word is brought from
the Williams memory to R^3 where it awaits further transfer. Set-up has
meanwhile enabled starting address recognition by the drum control.
Upon recognition of this address, a series of command signals developed
from permanent synchronizing marks on the drum is initiated. These
signals cause the word residing in R^3 to be transferred to ER, thence to
the drum via writing circuits.

When the desired number of such transfers has been accomplished
(EC is satisfied), one of two possible operations ensues. If a check of
the writing operation is desired, the above process is repeated except
that reading of the drum signals and comparison with the Williams infor-
mation is made. At the end of a successful check process the EC is once
more satisfied. At that time, or at the conclusion of the first cycle
if no check is requested, a termination signal is developed which causes
the computer control to terminate the first phase order it had originally
executed and to look at the second phase order, still residing in R_3.
This act returns the external control to an inactive state and transfers

the computer control to the next internally specified order, and normal computation resumes.

ii. Logical flow.

The preceding operations will now be described in greater detail and precise tracing of the sequence of events will be made. Reference to drawing #B-2556 will facilitate following the discussion.

The presence of the external execution order in R_3 and the subsequent $R_2 \longrightarrow R^3$ gate signal sets toggle $T_{GO\ AHEAD}$ (T_{GA}) to the on or 1 state. This toggle, signifying the presence of an external cycle when in this state, is turned off again only upon termination, i.e. completion of the external cycle and absence of the execution order "externa" digit. $T_{TEMPORARY}$ (T_T) has been in the off state, having been so set by the prior off state of T_{GA}. Gate 1 is therefore enabled and presents the priming word (which has just been transferred from R_2 to R^3) to the input of the ER. Gate 65, being open, allows an "into ER" gate command, and transfer into the register toggles is effected. After a suitable delay ($\approx$ 2 μs), delay #1 then enables gate 2 which produces a set-up command. This delay insures that the transferred digits will have had time to be stably stored in ER. Set up, coming on, disables the "into ER" gates via 65, so that the subsequent collapse of the enable DL signal will not put spurious information into ER. The set-up gate allows transfer of the 14 "# of events" digits to the EC via gate 46, the input gate system of the EC. The digits are inverted when transferred from ER to EC and then increased by one during the set-up operation, such that by adding a count of one for each subsequent information transfer, the EC will be fully loaded at the end of the required number of operations.

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INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.

EXTERNAL CONTROL

DRAWN: FEF   DATE: 9-15-55

SCALE: DWG. No. B - 2556

TOLERANCES UNLESS OTHERWISE SPECIFIED

FRAC:____ DEC:____ ANG:

Thus it will have a unique carry signal available out of the most sig-
nificant stage at that time.

Set-up also will turn on those send and receive toggles pertinent
to the operation. For the case of Williams to drum (i.e. writing on the
drum) the Williams send (2^{-34}) and drum receive (2^{-36}) digits are ones
in ER. Consequently gates 9 and 15 will operate, turning on T_{WS} and T_{DR}
respectively. Note that the conditions are also present on both gates
that $T_{DRUM\ CHECK\ 1}$ (T_{DC1}) is zero. This refers to the fact that the
present cycle is not a drum check cycle. It is seen that T_{WS} and T_{DR},
as well as other corresponding toggles for similar operations had been
set to the zero state when T_{GA} last went to the zero state.

The remaining digits present in ER, those defining the starting
address, are being statically presented to the drum address recognition
circuit. Delay #2, covering the set-up operation time, then presents a
command to T_{T}, putting it in the 1 state. This shuts off gate 1, then
gate 2, and the enabling of digit lines and set-up are both thereby
terminated.

Consider now the system involving Williams send and receive
toggles, drum send and receive toggles, etc. The outputs of these
toggles are mixed, through gates (11, 12, 16, 17, etc.) with two lines,
one marked send and the other receive. The states of these two lines,
(both are never "down" or "on" simultaneously) determine subcycles of
of activity interior to the larger, complete "external" cycle.

$T_{SEND/RECEIVE}$ ($T_{S/R}$) had been residing in the send state due to
the last turnoff of T_{GA}. The transitional inhibition into gate 7 re-
quires that the signal requesting setting of $T_{S/R}$ to S must have disap-

peared before the send line can be turned on. Since this signal is not now present ($T_{GA} \neq 0$) gate 7 is enabled as soon as T_T goes to the 1 state. Therefore after delay #2, the send line is driven down to the customary 1 (-30v) state. Since the only "send" toggle which had been turned on (at set-up) is T_{WS}, the only effect of being in the send state is enabling of gate 11.

An invitation to the computer for an action request is made by this gate, and the Y/0 toggle (turned off at the last memory sync time) is put in the 1 state, allowing the action request via gate 50. The Williams control is so organized that unless a specific request is made to write ($R_1 \longrightarrow M$), a reading or $M \longrightarrow R^3$ action will occur.

Upon the appearance of this $M \longrightarrow R^3$ signal, Williams places the requested word in R^3 and has done its sending. Hence the send portion of this minor cycle may be considered completed and a receive cycle is now in order. It must be recalled that since both the Williams memory clock period and the drum synchronizing pulses are independently derived and timed, a logical interlock between these two functions must be achieved. It will be seen now that the Williams memory having delivered its required word, will not be involved again until the drum can recognize its correct angular position, write the statically waiting word, then subsequently issue another action request if a new word is required.

If no drum check is in progress then the $M \longrightarrow R^3$ signal, enabling gate 5, puts $T_{S/R}$ into R. Again, with transitory inhibition (allowing the send line to be completely shut off), the effect of $T_{S/R}$ changing is not felt until the disappearance of the requesting signal. Gate 8 therefore enables the receive line as soon as the $M \longrightarrow R^3$ gate signal disap-

pears. The $M \longrightarrow R^3$ gate signal also causes the event counter to be stepped once.

As with the group of send toggles, only one receive toggle had been turned on at set-up time. This, since the drum is to receive, is T_{DR}. With the receive line on, gate 17 is enabled and now the request for drum recognition is made.

The details of drum recognition will be described in the section under drum logic. It is sufficient for the present discussion to point out that the request for recognition is initiated at gate 32, and upon recognition two events occur. First, gate 36 is enabled which in turn provides gating of the signal from R^3 into ER, making available in ER the word to be written on the surface of the drum. Second, gate 34 will be enabled by the desired drum sync pulse, and since $T_{DR} = 1$, gate 37 will be enabled for the duration of that pulse, ≈ 2 μs. This signal, $ER \longrightarrow D$ commands the drum writing circuits and effectively transfers the word in ER to the drum surface. The required operation has now been accomplished and it remains to either terminate the cycle completely, check the writing operation if requested, or initiate another minor loop and word transfer if the required number of events has not occurred. The $ER \longrightarrow D$ signal turns on $T_{TERMINATE}$ which had been set to zero the last time $T_{S/R}$ was in the S condition. Gate 57 therefore is enabled and gates 38 and 39 therefore are potentially enabled. Suppose that the preceding operation had been one of several requested, and that further words remained to be written on the drum. In that case there will be no carry in the EC, and gate 39 will be enabled. This will set $T_{S/R}$ back to S, and then the process just described will be repeated with the suc-

ceeding word in the Williams memory being written. Suppose however that
the word just handled represented the final word to be transferred.
There will then be a carry signal out of the EC, and gate 38 will be
enabled. Now two choices are present. Assume first that no check is
desired. In that case neither gates 59 nor 60 will have been enabled
and since this is not a graphing operation, gate 55 will not have turned
T_D, on at set-up. Consequently a signal out of 38 will issue a termina-
tion order to the computer control, closing the computer order gates.
Gate 38 (via gate 54) also will issue a down' order to the computer con-
trol, causing it to advance to the ϕ_2 order, the previously mentioned
transfer control order in the second phase of the execute order-pair.
With the advent of the termination process, the external digit in the
first phase goes to zero, turning off T_{GA} which in turn collapses the
entire external control set-up, returning it to a quiescent "off" state.

Consider now the remaining case, drum check. The drum check pro-
vision allows a digit for digit equality check of either reading or
writing operation. Checking is made at the option of the operator and
is called for or inhibited by manual switching at the operating console.
Both "check read" and "check write" are similar procedures. After the
full transfer of words called for, the cycle is repeated except that for
check write the drum is read out, word by word, and comparison made in
the adder of the computer with the presumably identical information
stored in the Williams memory. The checking process will hang up at the
first discrepancy and the operator must manually reset an error toggle
in order to proceed. The Williams word involved is displayed in R^3 while
the corresponding drum word appears in R_1 and the discrepancy may be

easily noted.

Suppose that a write check had been desired. Since the drum-receive digit (2^{-36}) had initially been present in ER, gate 55 at set-up time will have put $T_{D'}$ in the 1 state. This inhibits gate 54 so that the Down' signal is not developed at the end of the full writing cycle. A termination signal is, as before, sent out. This has the effect of turning off T_{GA} and resetting the external control to the quiescent condition. However, this results in $T_{S/R}$ being set to S which has the property of setting T_{TERM} to 0, thus removing the termination request. Since no Down' order has been given, the computer control thus sees the first phase order all over again, and T_{GA} is turned on, beginning a new external cycle. This time, however, the signal out of gate 38 had provided a condition which was not present at the beginning of the initial cycle. Gate 41 is enabled and $T_{DRUM\ CHECK\ 1}$ (T_{DC1}) is turned on. Note that it was guaranteed to be off by the last Down' signal.

$T_{DC1} = 1$ now sets up the drum check operation. Note that the priming word cannot set T_{WS} and T_{DR} as before since the gates involved for this operation depend on $T_{DC1} = 0$. Instead, T_{DS} and T_{WR} are turned on by virtue of $T_{DC1} = 1$. The drum as sender in this case is legitimate, since we wish to read from the drum. Williams is to be the receiver, but not in the usual sense. Since no explicit command for writing in Williams is generated, it will still read out into R^3 when an action request is received. It is now necessary to bring the two presumably identical words into the adder and to compare them.

At set-up gate time, gate 56 is enabled by T_{WR} coming on $(T_{S/R} = S)$. This clears R_1 to all zeros preparatory to reception of the

drum word.

T_T going to the 1 state produces two effects. The send line is enabled causing gate 16 to initiate a recognition request. Meanwhile the gated outputs of the drum signal amplifiers have been enabled (by $T_{DS} = 1$) preparatory to reading out the desired information. The other function of $T_T = 1$ is to null the complement gates of the adder in the computer, disabling any undesired carry in the adder. After recognition by the drum circuitry and the subsequent delivery of read out pulses, $D \longrightarrow ER$ via gate 35, information transfer may proceed. Each $D \longrightarrow ER$ pulse (≈ 1.5 μs shaped drum sync pulses) produces an into ER gate. Since the drum amplifier output gates are open, this effectively places the read out drum information into ER. The first $D \longrightarrow ER$ signal will set T_X to the 1 state, and since T_{DC2} and T_{DC3} are still off, this will advance the event counter and set $T_{S/R}$ to R. Gate 66 is thereby disabled, turning off T_X which removes the request for $T_{S/R} = R$. The receive line is enabled and three events ensue. First, an action request $(M \longrightarrow R_3)$ is made. Second, the information is gated from ER into R_1 via gate 52. Third, gate 40 is potentially enabled, but since $T_{DC1} \neq 0$, is not operated.

When the computer delivers the required word from Williams to R^3, the $M \longrightarrow R^3$ gate enables gate 43 and T_{DC2} is turned on.

Consider now that the word brought from Williams is being statically presented to the adder via the complement gates (from R^3) and the word brought from the drum is being presented to the other side of the adder via R_1. With the end of the $M \longrightarrow R^3$ gate, gate 3 is enabled and produces a minus complement gates signal as well as potentially

enabling gates 44 and 45. A carry of 1 will be produced in the 2^0 stage of the adder if the two numbers are equal, or if one or more superfluous ones are present coming into the adder. If, however, there are insufficient ones or excessive zeros, the carry will never be produced and the cycle will go no further. If the first condition is met, the eventual carry out of the 2^0 stage will enable gate 44, turning on TDC_3. This in turn removes the injected 2^{-39} carry from the adder. Now, if excessive ones are present in either word, a 2^0 carry will still be produced. If and only if the two words are identical will the 2^0 carry collapse.

Thus the cycle proceeds for a successful 2^0 carry = 0 since gate 45 will now be enabled. Once again inspection is made of the state of carry in the event counter. If it is required that more words are to be checked, then the minor cycles proceed as before. If the EC is satisfied, then a termination signal is produced. Since $T_{D'}$ has been turned off by T_{DC2} = 1, gate 54 makes possible a down' signal. Hence the cycle is completely terminated and the computer will proceed with the second phase order.

iii. Circuits.

1) External Register - Dwg. #A-2554.

The external register is a full 40-stage parallel register which has been presently provided with four inputs. Incoming digits from R^3 are admitted and digit line disconnection insured, when desired, by a local gate. The gated output of the R^3 signals is diode mixed with the drum, tape, and IBM inputs. Other input provision for future expansion may of course be easily added.
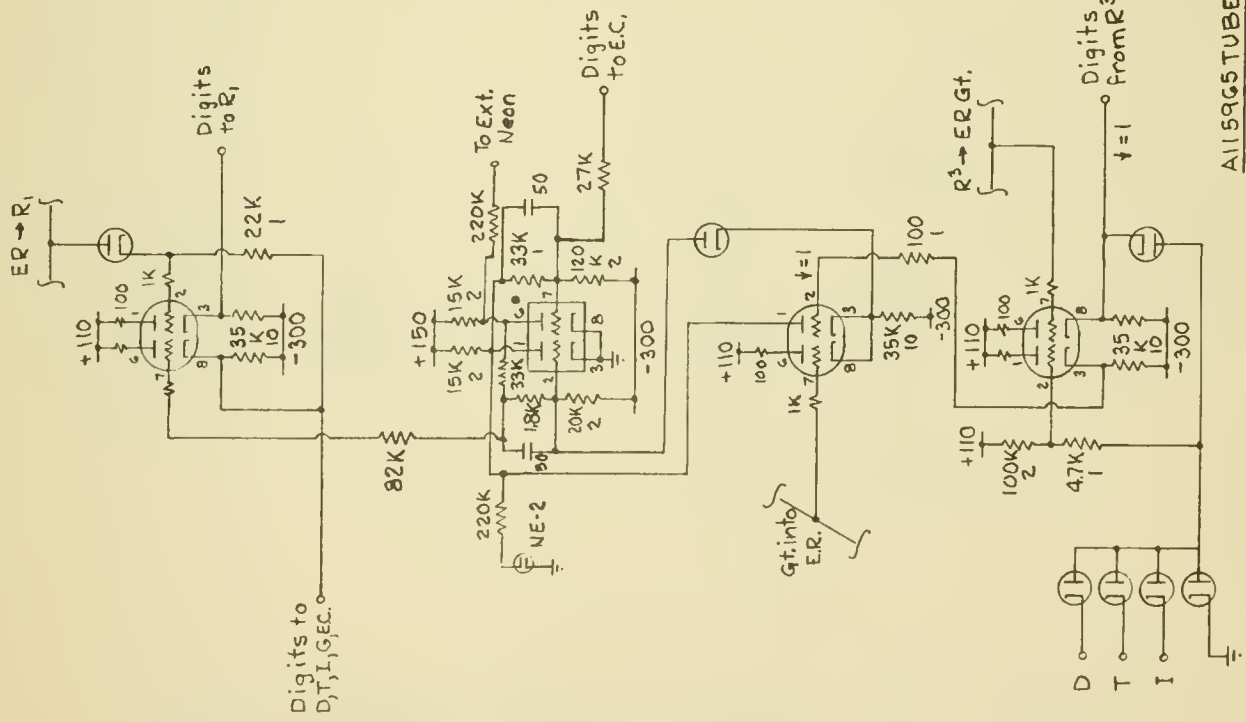
ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N.J.

EXTERNAL REGISTER

DRAWN: F. Fell   DATE: 10-5-55

SCALE: Dwg. No. A-2554

All 5965 TUBES

ELECTRONIC COMPUTER PROJECT
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PRINCETON, N. J.

EVENT COUNTER

Drwn F.Fell
Date 10-3-55

DwgNo. A-2553

All Toggles as shown.
↑ Voltage =+110v.; ↓ = -300v.
All tubes are 5965 except
as marked.

Digits In

1st Stage

7th Stage

Carry In

Carry Out

Into Ec Gate

Gec → Ecl

Note:
1 Voltage = ±10 volts, 0 voltage = +300 volts
Grid suppressors are 1K, plates and anodes
All tubes are 5915's, diodes Hughes 1N81
Neon wiring for toggles as shown below.

That set of input digits being received is gated into the ER toggle via a conventional double sided gate at the command of the $\longrightarrow$ ER gate signal. The double sided gate was considered preferable to a single sided system in order to reduce circuit complexity and to avoid time required for clearing.

Speedup condensers across the ER toggle crossover resistors were employed to insure a stable state of the toggle for the relatively short gating time when reading. (D $\longrightarrow$ ER $\approx$ 1.5 μs.)

The 14 stages of ER which connect to EC feed their signals directly from the ER toggles. All stages of ER communicate the states of their toggles to the drum, tape, IBM, graphing, etc. via a cathode follower which also presents these digits to R_1 through the mediation of the ER $\longrightarrow R_1$ gate.

2) Event Counter - Dwg. #A-2553.

The event counter is a 14 stage half-adder type counter of the same type as the dispatch counter used in the main machine. The upper rank of toggles of this counter are primed by the inverted digits of the proper stages of ER at set-up gate time. As described in section b.ii. each minor cycle of the control will add one more count to the EC until a full count of 1's in each stage has been achieved. At that time a unique carry signal out of the most significant stage of the EC will be produced.

3) Control - Dwg. #B-2555.

The circuit realization of the control is essentially a straightforward representation of the logical system described in section b.ii.

Toggles and gates are of the same design used throughout the main computer with one exception. No vacuum diodes were employed; germanium diodes were used exclusively.

The two delay circuits required consist of two triode inverter sections each with a capacitor on the grid of the second section. Thus for a down going signal on the first grid, the capacitor following its plate crossover resistor must charge up before the second grid rises enough to bring the second triode section out of cutoff. Therefore the second plate will produce a down going signal only after a delay measured by RC, where R is the equivalent resistance seen by the second grid. The converse will be true for an up-going signal.

    c. New drum.

       i. Overall function.

An ERA type 1107 drum was purchased, adding a potential of 16,384 words (40 bits each) of medium speed memory to the computer system. Any number of or all tracks (each track 4096 words) may be preserved, i.e. no subsequent writing permitted. Reading, however, is never inhibited. The average access time (to begin any operation) is 17 1/2 milliseconds.

The topological organization of information on the drum surface is as follows:

TRACK 00(A)	TRACK 01(B)	TRACK 10(C)	TRACK 11(D)
40 BIT WORD	40 BIT WORD	40 BIT WORD	40 BIT WORD
4096 WORDS	4096 WORDS	4096 WORDS	4096 WORDS

Since the rotational period is $\approx$ 35 milliseconds, and there are 4096 words presented during this time to any one track, the average rate of information flow is $\approx \dfrac{35 \times 10^{-3}}{4.1 \times 10^{3}} \approx$ 8.5 microseconds. The basic Williams clock cycle, defining repetetive access gime from that store is from 20 to 25 μs. and therefore is too slow for the drum bit repetition rate. The drum check cycle imposes additional time requirements on the machine period (more time required for two carries plus logical operations). It was decided then to provide an interlace of 8 to 1, that is to use every eighth word in sequence on the drum. This produces a repetition rate of $\approx$ 8.5 x 8 = 68 μs. which is sufficient time to allow a full Williams cycle plus the additional operations.

Two sets of sync tracks are employed to provide a constant knowledge of the drum's angular position and to synchronize reading and writing operations. There are 4095 (0-4094) "S" marks on one track, $\approx$ 8 μs. apart and one "0" (origin) mark (8 μs. after mark #4094) on the other track. The drum periphery may be divided into 4190 equal intervals, therefore there are 94 intervals not used. Consequently an unused gap (known as the origin gap) exists between the "0" pulse and the beginning or #0 "S" pulse.

A 12 stage counter (θ counter) is employed to count both S and 0 pulses, hence is fully loaded after 4096 counts. A two stage counter (track counter) is used to select any one of the four sets of tracks (40 channels per set). This counter derives its initial input information from the two most significant digits of the starting address (2^{-1} and 2^{-2}). A three stage interlace counter provides an output for each eighth input, thus changing 8 μs. pulse sequences into 64 μs. intervals, the basic

period for drum information transfer.

Writing of signals on the drum is accomplished by saturation of the oxide surface which has originally been erased to a neutral state. The second loop of the read back signals is strobed to obtain either a + or - output signal (- for 1, + for 0) and processed by 40-gated feedback amplifiers.

ii. Logical flow.

In section b.ii. a description of a drum writing sequence was given. Let us return to the point where recognition has been requested. Reference to drawing B-2556, External Control, will facilitate following the present discussion.

Gate 32 will be enabled with the presence of any 8 us. sync pulse (either "S" or "O"), turning on $T_{RECOGNITION\ PERMIT}$ $(T_{REC.PER.})$. Meanwhile the θ counter has been continuously indicating the angular position of the drum, being advanced one count for each S or O pulse. This count in the θ counter is statically presented to a coincidence recognition circuit which has for its other input the starting address residing in ER. When both numbers are identical, the coincidence circuit develops a recognition signal, called θ satisfy, and the drum is then at the desired position for information transfer. To insure a stable, unchanging θ count and therefore an unchanging θ satisfy signal, gate 33 is enabled only after the 8 μs. drum sync producing $\theta_{SAT.}$ has disappeared. This turns on $T_{RECOGNITION}$ $(T_{REC.})$. The on state of this toggle defines the act of recognition; its output then is known as post recognition. It is that signal which, as indicated in section b.ii., enables gates 36 and 34.

Provision has been made for detection of an error in the θ
counter such that once each drum revolution, accuracy of the θ count is
tested. If this count is in error, gate 34 will be disabled and further
information transfer may not proceed until a toggle has been manually re-
set.

The details of the θ error circuit are seen in the Drum Control
drawing #0-2557 in section c.iii.12. A full count in θ ($4095 \longrightarrow 4096$ carry)
will occur at a proper time only when the corresponding carry into θ has
resulted from the end of the last "S" pulse preceding the "0" pulse. In
that event, gate 61 will remain disabled when the "0" pulse appears.
However, if θ carry should not appear at this precise time (corres-
ponding to an error in the θ count) then gate 61 is enabled at "0" time
($T_{ORIG\ 1}$ being off), and $T_{ORIG\ 2}$ is turned on. This in turn turns on
T_{ERROR}, inhibiting further operation until $T_{ORIG\ 2}$ is manually reset.

The θ counter is reset to zero in all stages at "0" time, but for
correct counting this is a redundant operation. Since during turnon of
the equipment an error in θ is probable, $T_{ORIG\ 2}$ is automatically reset
by the computer's Williams charging operation, a process which occurs at
each turnon.

If no error is present, gate 34 will be enabled with each inter-
laced sync pulse, i.e. pulses occurring every 64 μs. These pulses then
are used to drive either the write amplifier (pulse shaper) or read
amplifier as required.

The track counter, having been initially primed with the correct
starting track information (00 = A, 01 = B, 10 = C, 11 = D) at set-up
time, has selected the desired group of 40 heads. Each time the last

BY ....JP.... DATE ....
CHKD. BY ...... DATE ....
25 Oct 55

SUBJECT ....
Drum Timing Control

SHEET NO. ...... OF ......
JOB NO. ....

* Gate drivers and carry exclusion circuits needed here

Set up gate

Starting Track

Track ctr   2 stage

Select Track

S

T_REC = 1

Interlace Counter 3 stage

Clear → 1: at Set up Gate

111 count

Thru origin

O

T_REC = 1

S + O

8 µs sync

O

Manual reset or Vws change

origin check

Carry 4096 → 4096

S

Starting Address

Coincidence Circuit

θ counter (12 stages)

T_CA = 0

O

Terror

Satisfy

34

34

64 µs sync

D_R

17   RECEIVE

D_S

16   SEND

32

S + O
(8 µs sync)

T_CA = 0

T_RECper

$\overline{S+O}$

T_CA = 0

O

T_Rec

36

Read Pulser

D_S = 1

35

D → ER

Write Pulser

37

D_R = 1

ER → D

Drum Timing Control
25 Oct 55   JP
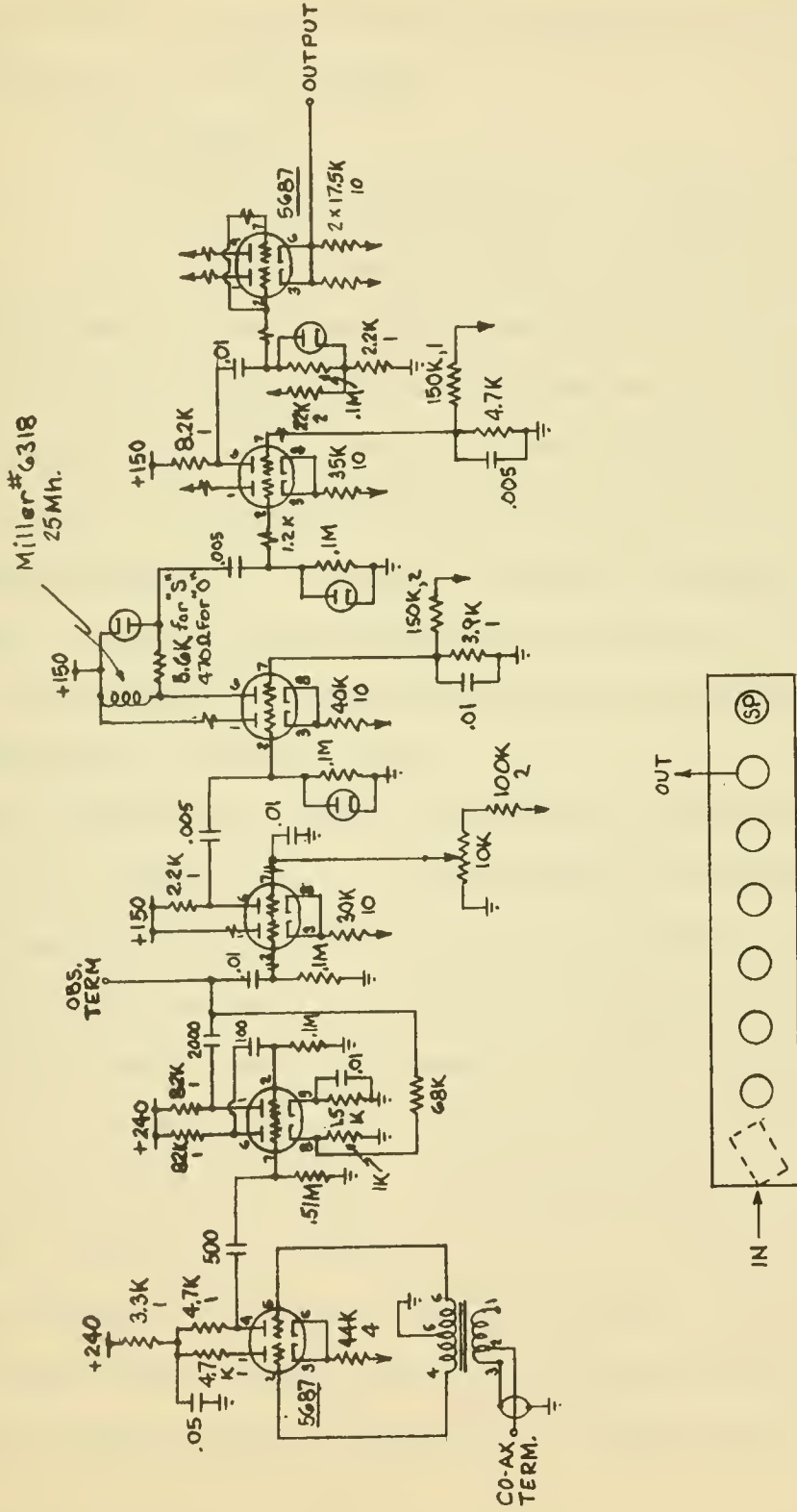
Miller #6318
25 Mh.

5487

2 × 17.5K
10

OUTPUT

+150

8.2K

.01

1.2K

.IM

.01

2.2K

.IM

150K, 1

4.7K

.005

35K
10

.005

8.6K for "S"
470Ω for "0"

+150

40K
10

.IM

150K, 2

3.9K
1

.01

.01

.IM

+150

2.2K .005

30K
10

10K

100K
2

OBS.
TERM.

.01

.IM

82K
1

2000

100

.IM

.01

+240

82K
1

.15
1
K

1K

68K

.51M

500

+240

3.3K
1

4.7K
1

47
K

5487 3

44K
4

.05

.6

.1

CO-AX
TERM.

Note:
↑ Voltage = +110 v., ↓ = -300 v.
Plate suppressors = 100Ω, grids = 1K
All tubes are 5965 except as noted.
All diodes are Hughes 1N117.

SP

OUT

IN

word in any one track has been used this counter will be advanced to the next higher count, or successive track. At present, since only 120 heads or 3 tracks are used, the selection has been arranged to switch to track A following track C; D not being used.

iii. Circuits.

1) Drum sync amplifiers (S & O pulsers) - Dwg. #A-2563.

The "S" and "O" pulsers are identical except for differing damping resistances in the ringing coil circuit. The sync signals as read back from the drum are sinusoidal and must be amplified and shaped, care being taken to insure accurate repetition of timing.

A single stage of balanced amplification driven from a 30 turn center tapped secondary of an ERA head transformer comprises the input stage. This is followed by two stages of RC feedback amplification. Up to this point the circuit is essentially the same as that of the main drum signal amplifier. (Dwg. #A-2564.)

This is followed by a cathode follower gate, serving to square up the sync signals, using a bias level sufficiently close to ground to catch the steepest slope of the input signal (thus insuring good repetitive timing), yet sufficiently off ground to be insensitive to small noise voltages. The following stage employs a cathode coupled gate with a ringing coil in its plate circuit. Choice of L (and distributed C) provides a signal of desired width. Critical damping and a positive acting bumper results in the production of a 60-70 v. steeply falling signal of controlled width for each input sync signal. Final processing involves another cathode coupled gate for sharpening and squaring this pulse, and a cathode follower to provide a low impedance source to dis-

tribute the "S" or "O" pulses.

   2) Read amplifier (pulser) - Dwg. #A-2572.

Since the signals supplying both read and write pulsers are the typical 0-30 v. logical signals, no preamplification is required. In order to strobe the second loop of the read-out drum signals, a sync delay of half a period ($\approx$ 4.2 μs.) is required. The input to the read amplifier then is delayed by this amount by a fixed, low impedance delay line. The circuit of this pulser is essentially the same as that of the "S" and "O" pulsers just described. The output signal, D $\longrightarrow$ ER is required to be quite crisp in order to insure the fastest possible gating of the read out signals into ER, hence is driven by 4 full 5687 cathode followers.

   3) Write amplifier (pulser) - Dwg. #A-2578.

This pulser is similar to the preceding one in most respects. Note that both read and write pulse widths are adjustable (variable ferrite core L's) in order to allow optimizing adjustments.

Under some conditions of equipment turnoff and in particular, turnon, spurious write pulse (ER $\longrightarrow$ D) signals could be generated. For example since B+ turnon is sequenced (first + voltages then - voltages are applied) a transient in +110 or +150 could momentarily drive the write sync output negative, causing random signals to be written inadvertently on the drum. Also, since -300 undergoes a fairly large transient perturbation during turnon, this too could result in spurious writing. Consequently a filtered holdoff voltage is used to hold up the output, insuring no writing, until a guaranteed time after -300 makes its appearance, energizing the relay which had held up the
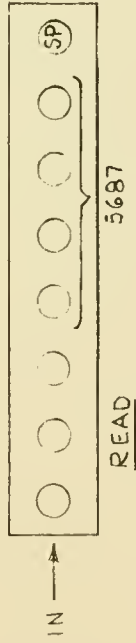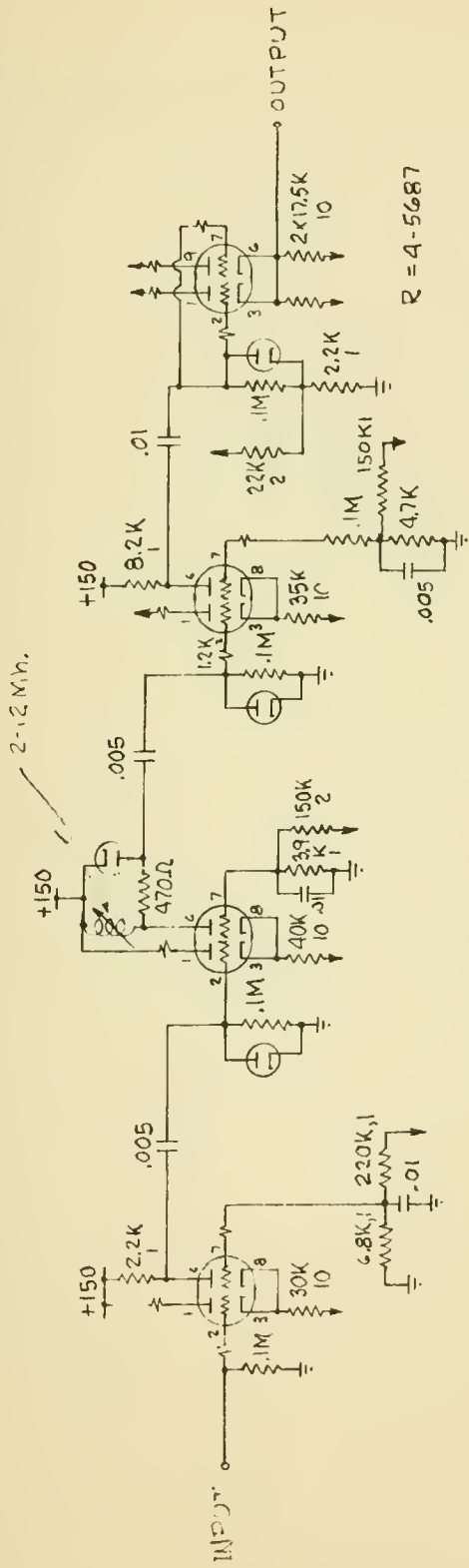
OUTPUT

R = 4-5687

INPUT

2-12 M.h.

READ
5687
(SP)

IN

Note:
Voltage = +110V., ⅄ = -300v.
Plate suppressors = 100Ω, grids = 1K.
All tubes are 5965 except as noted.
All diodes are Hughes 1N117.

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INSTITUTE FOR ADVANCED STUDY
PRINCETON, N.J.

READ AMPLIFIER

DRAWN: F. Fell | DATE: 1-17-56

Dwg. No. A-2572

SCALE:

ELECTRONIC COMPUTER PROJECT
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PRINCETON. N. J.

WRITE AMPLIFIER

DRAWN: F. Fell | DATE: 6-12-56

SCALE: | Dwg. No. A≡2578

Note:
↓Voltage = -300v. ↑ = +110v.
Plate suppressors = 100Ω, grids = 1K.
All tubes are 5965 except as noted.
All diodes are Hughes 1N117.

5687

IN →

INPUT

OUTPUT

output cathodes.

          4)   Write gate drivers - Dwg. #A-2562.

          The organization of the drum reading-writing system requires that 40 parallel digits be handled simultaneously. It is required therefore that for writing, 40 pulser tubes, driving the drum heads, be gated at write sync time. Forty drivers then, gating these pulser tubes, are provided, driven by driver drivers (to minimize loading effects of the multiple grid input capacitances), which are in turn driven by the write pulser just described.

      The gating system has been split into two halves, 0-19 and 20-39 to provide half word operation if desired, but no use is at present made of this provision.

          5)   Drum amplifier - Dwg. #A-2564.

          There are 40 plug-in amplifiers which may be electronically switched to either of the four tracks (see the following section, c.iii.6) to select 40 heads either for reading or writing. The same transformer is used for both operations, so the transformer primary connections represent a common point which is the input of the read amplifier as well as the output of the write pulser tube.

      Writing on the drum is accomplished by presenting the desired information digit from ER, via the digit repeaters (see section c.iii.7) to one grid of the 5687 pulser tube. Its other grid is provided with the inverted digit. Hence for a 0, one grid will be at gound and the other at -30 v., while the potentials are interchanged for the 1 case. At write sync time, the write pulser via the previously described write gate driver, pulls down the cathodes of the pulser tubes, passing
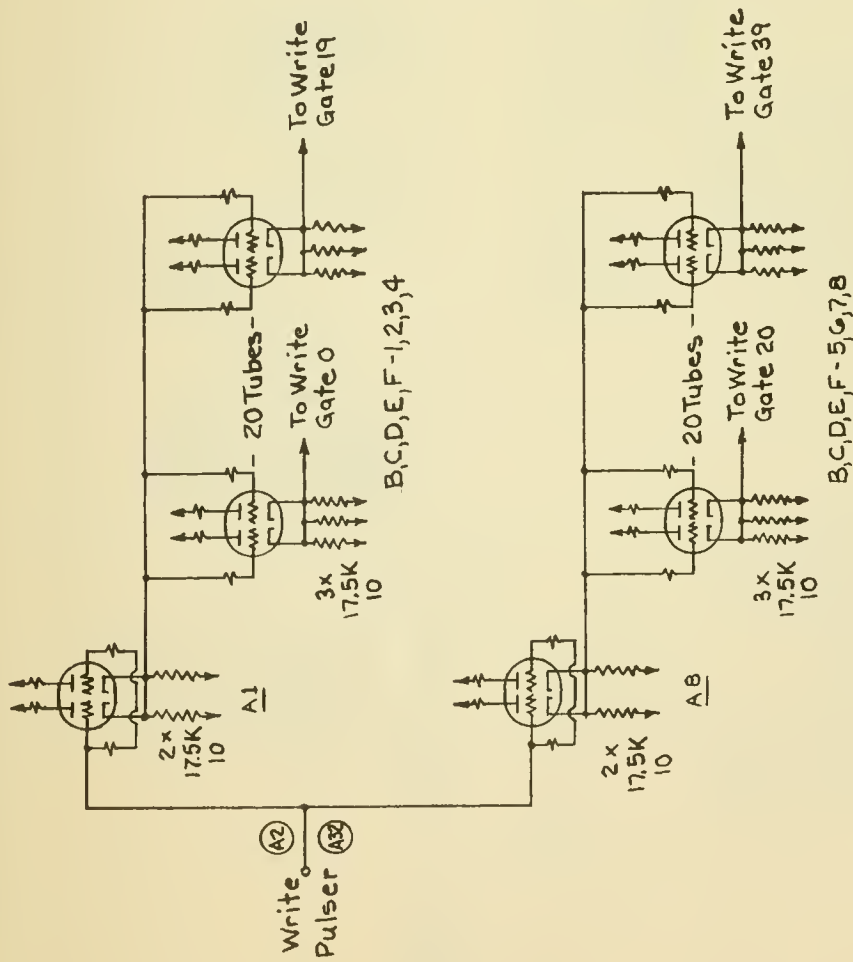
STAGE	TUBE	TERM	STAGE	TUBE	TERM
0	B1	A1	20	B5	A17
1	C1	A3	21	C5	A19
2	B2	A5	22	B6	A21
3	C2	A7	23	C6	A23
4	B3	A9	24	B7	A25
5	C3	A11	25	C7	A27
6	B4	A13	26	B8	A29
7	C4	A15	27	C8	A31
8	E1	G1	28	E5	G17
9	F1	G2	29	F5	G18
10	D1	G3	30	D5	G19
11	E2	G5	31	E6	G21
12	F2	G6	32	F6	G22
13	D2	G7	33	D6	G23
14	E3	G9	34	E7	G25
15	F3	G10	35	F7	G26
16	D3	G11	36	D7	G27
17	E4	G13	37	E8	G29
18	F4	G14	38	F8	G30
19	D4	G15	39	D8	G31

To Write Gate 19

To Write Gate 0

B,C,D,E,F-1,2,3,4

20 Tubes

To Write Gate 39

To Write Gate 20

B,C,D,E,F-5,6,7,8

20 Tubes

3x 17.5K 10

A1

2x 17.5K 10

3x 17.5K 10

A8

2x 17.5K 10

Write Pulser (A2) (A32)

Note:
Voltage = +110v., = -300v.
Plate suppressors = 100Ω,½ Grids = 1K, ½
All tubes are 5687

Note:
↑ Voltage = +110, ↓ = −300
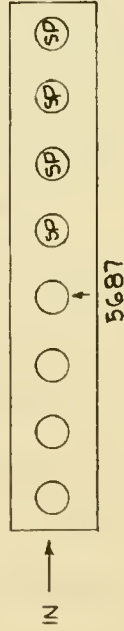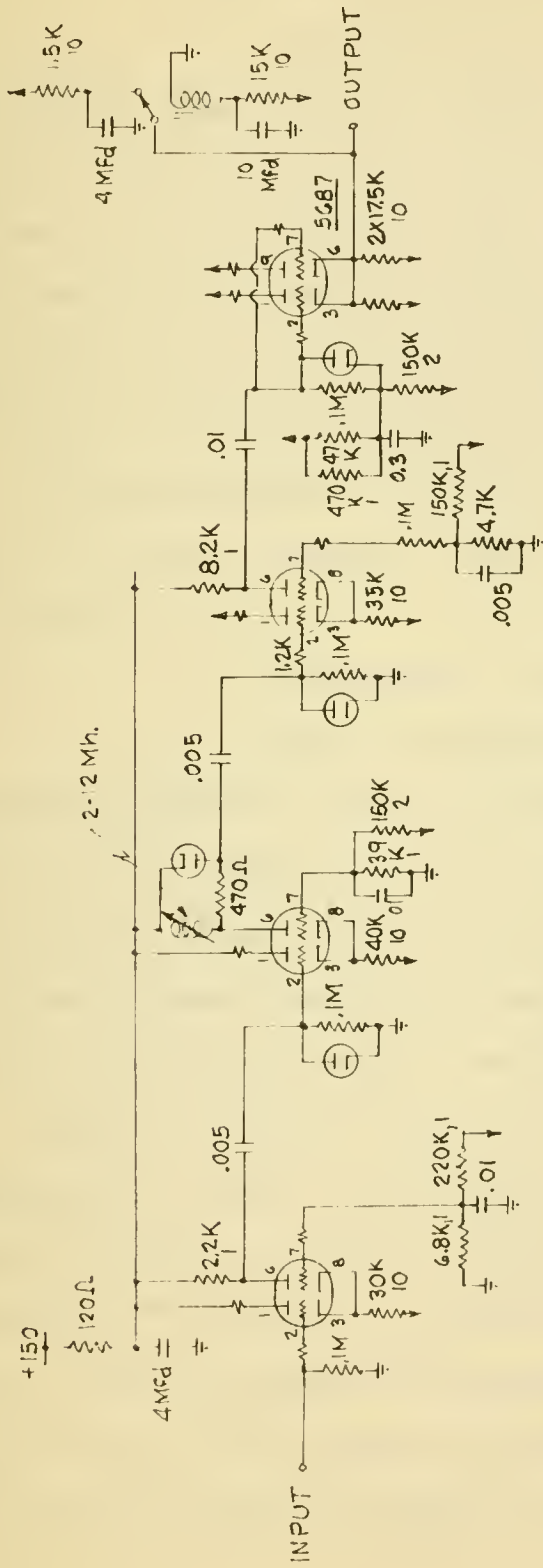Plate suppressors = 100Ω, grids = 1K
Tubes are 5965 except as noted.

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INSTITUTE FOR ADVANCED STUDY
PRINCETON. N.J.

DRUM AMPLIFIER

DRAWN: F.Fell | DATE: 1-4-56

SCALE: | DWG. No. A-2564

current through the transformer primary in the desired direction and writing on the drum through the head connected to the secondary of the transformer. A spurious signal is developed in the read amplifier at this time, but since no reference is being made to its output, it is of no consequence.

For reading from the drum, the transformer secondary is presented to the push-pull input stage. This stage and the two stages of feedback RC amplification following are identical to the input stages of the drum sync amplifier previously described.

Output signals, on the order of 100 v. peak to peak appear at the output gate, to be cathode followed out during reading by the presence of the negative going gate signal, drum read permit, developed in the drum control circuit. (See section c.iii.12.)

The reference level about which these signals vary is known as the read amplifier bias and is controlled in common with the other 39 stages to provide optimized gating into ER.

6) Diode-transformer chassis - Dwg. #A-2577.

Each of the 40 amplifiers was shown to have its input connected to a single transformer primary. This is now seen to be a simplification of the actual case. Since there are potentially 160 heads in 4 groups and only 40 amplifiers, it is required that each amplifier be potentially connectable to one of four transformers at will.

Any one amplifier then, is connected to a pair of busses which are diode connected to 4 transformer primaries. If B+ is applied to only one primary center tap and the other center taps are held slightly

To Drum Head & Erase Circuitry
(Grouped in sets of 10 - See dwg A·256B)
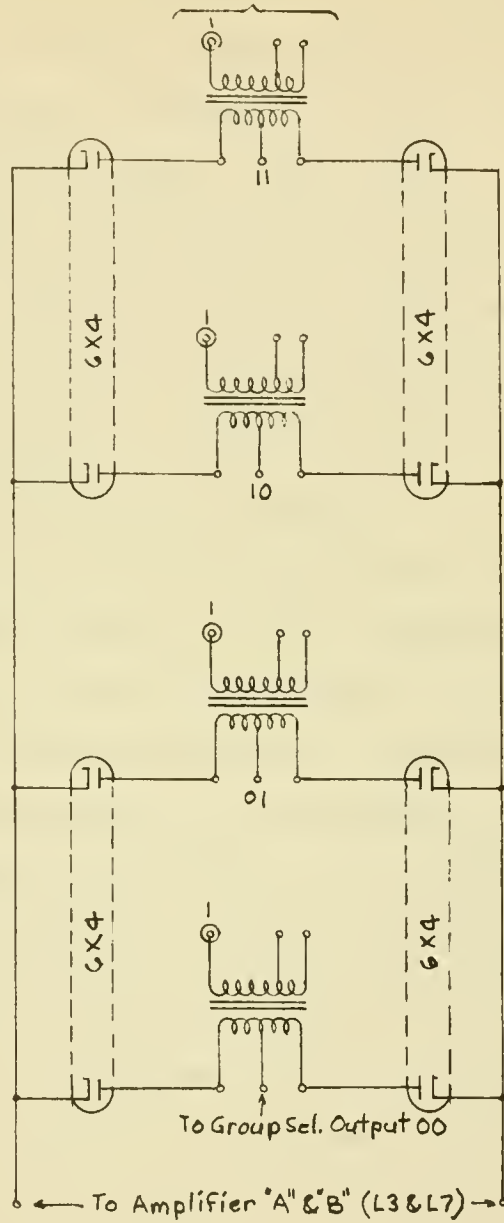
11

10

01

To Group Sel. Output 00

←—— To Amplifier "A" & "B" (L3 & L7) —→

6X4   6X4   6X4   6X4

negative, then the diodes will connect only the desired transformer and head to the amplifier. Thus by switching the 4 B+ voltages, track selection is accomplished and only 40 rather than 160 amplifiers are required. This track selection is described in section c.iii.8.

7) Digit repeaters - Dwg. #A-2567.

The primary function of the digit repeaters is to provide a local cathode follower for each digit fed to the drum pulsers during writing (thus minimizing the load of cabling already present on the cathode followers in ER) and to isolate the effect of changing ER information on the amplification during reading.

There are 40 single sections of cathode followers which present the ER digits to the pulser grids for writing. During reading, however, even though the nulled write gate inhibits current flow in the pulser tube, some grid-plate capacitance effects and a small but finite amount of conduction will couple ER signals into the amplifier input. Since the ER information is changing due to the act of reading, a feedback loop is possible; introducing noise and spurious read signals. To inhibit this effect, the digit repeaters are held off by an inverted read permit signal. This is the same signal which gates the amplifiers' output. Thus for a read command, the digit repeaters are made insensitive to ER information (their grids are held at $\approx + 8$ volts) and there is negligible coupling of changing ER information into the read amplifiers.

8) Track selector matrix and group selector - Dwg. #A-2569.

The digits from the two stage track counter are fed from the upper row of toggles of that counter to a matrix which subtracts one from the count and provides the proper input voltage levels

+150
15K
33K
1K
100
↓ Drum Read Permit Left Drum Control C3
10K
1K
C3
35K,10
C3 120K
5965

+110
100
1K
D5 D6 D7 D8
5965's

2×35K,10
-300
↑ = Read

	1	2	3	4	5	6	7	8
A	O	O	O	O	O	O	O	O
B	O	O	O	O	O	O	O	O
C	O	O	O	O	O	O	O	O
D	O 32,33	O 34,35	O 36,37	O 38,39	O	O	O	O
E	O 16,17	O 18,19	O 20,21	O 22,23	O 24,25	O 26,27	O 28,29	O 30,31
F	O 0,1	O 2,3	O 4,5	O 6,7	O 8,9	O 10,11	O 12,13	O 14,15

2^n IN
22K
100
22K
2^m IN
2^n OUT To Amp.
35K 10
2^m OUT To Amp
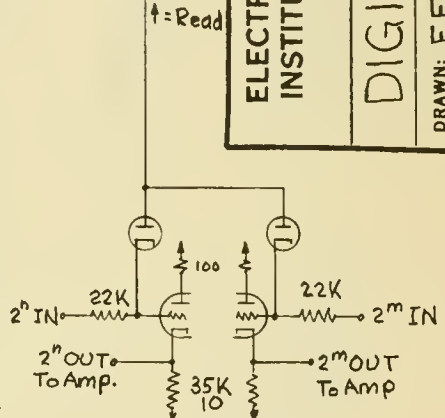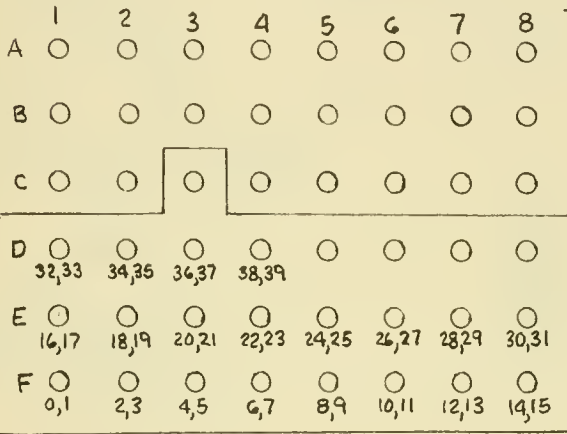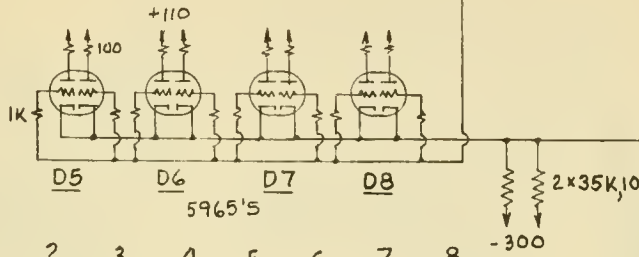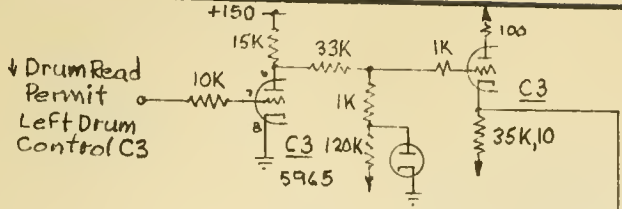
40 Stages
(20 Tubes) 5965

TUBE	DIGIT	TERMINALS IN	OUT	TUBE	DIGIT	TERMINALS IN	OUT
F1	0 / 1	I2 / I3	I1 / I4	E3	20 / 21	H10 / H11	H9 / H12
F2	2 / 3	I6 / I7	I5 / I8	E4	22 / 23	H14 / H15	H13 / H16
F3	4 / 5	I10 / I11	I9 / I12	E5	24 / 25	H18 / H19	H17 / H20
F4	6 / 7	I14 / I15	I13 / I16	E6	26 / 27	H22 / H23	H21 / H24
F5	8 / 9	I18 / I19	I17 / I20	E7	28 / 29	H26 / H27	H25 / H28
F6	10 / 11	I22 / I23	I21 / I24	E8	30 / 31	H30 / H31	H29 / H32
F7	12 / 13	I26 / I27	I25 / I28	D1	32 / 33	E2 / E3	E1 / E4
F8	14 / 15	I30 / I31	I29 / I32	D2	34 / 35	E6 / E7	E5 / E8
E1	16 / 17	H2 / H3	H1 / H4	D3	36 / 37	E10 / E11	E9 / E12
E2	18 / 19	H6 / H7	H5 / H8	D4	38 / 39	E14 / E15	E13 / E16

G
H
I

Bottom Terminal Strip

ELECTRONIC COMPUTER PROJECT
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PRINCETON, N.J.

TRACK SELECTOR MATRIX &
GROUP SELECTOR

Dwn: F. Fell   DwgNo. A-2569

Date 1-16-56

GROUP SELECTOR
CHASSIS

ONDIGIT REPEATER
CHASSIS

Note:
↑ Voltage = +110v, ↓ = -300v.
Plate suppressors are 100Ω, grids are 1K.

To C.T. of Transformers Group A

To Ext. Neon

to the group selector. The reason for subtraction of one is as follows.
Consider for example 00 (Track A) called for by the ER digits. At set-
up gate time this information is gated into the upper two toggles of the
track counter as 00. Set-up also produces an internal gate, setting the
lower rank to 00, and disappearance of set-up produces a carry which then
gates a one into the 2^0 upper toggle. Thus after set-up, the upper rank
holds 01, which is one more than the 00 originally required.

Subtraction of one is accomplished by the track matrix configura-
tion. Also, for the present, whenever group D is selected, group A is
enabled. This allows continuous sequential track selection until such
time as the 40 heads for track D are installed.

The group selector is an electronic switching device for providing
rapid and noise free B+ supply to the head transformer centertaps. Since
writing current (including losses) in the primary is required to be
≈ 50 MA., it is necessary to supply 40 x .05 or 2 amperes to the 40 se-
lected channels at +180 v. and to supply -20 volts to the three unse-
lected groups (120 channels).

9) Drum erase - Dwg. #A-2568.

Provision for erasing the drum in multiples of
groups of 10 tracks in any one group is an integral part of the equip-
ment. It is only required to plug in a variable amplitude 60 ~ source
of 6 volts at $\geq$ 10 amps. RMS. This is done by a motor controlled variac
connected to a bank of current metered filament transformers. Erasure
is accomplished by turning up the variac manually until a maximum of
1A. RMS flows in a single head, then allowing the motor drive to slowly
reduce the current to zero. This is done in ≈ 45 seconds.

APPLY
AC ERASE

ERASE

USE

To 15 Groups
of 10 Stages

.01

1Mh.

.01

TRANSFMR.

33Ω

HEAD

10 Stages

TRANSFMR.

33Ω

.01

1Mh.

.01

HEAD

R.F.Connector
& cable

USE

ERASE

To 3 Groups
of 4 Sets

4 Sets
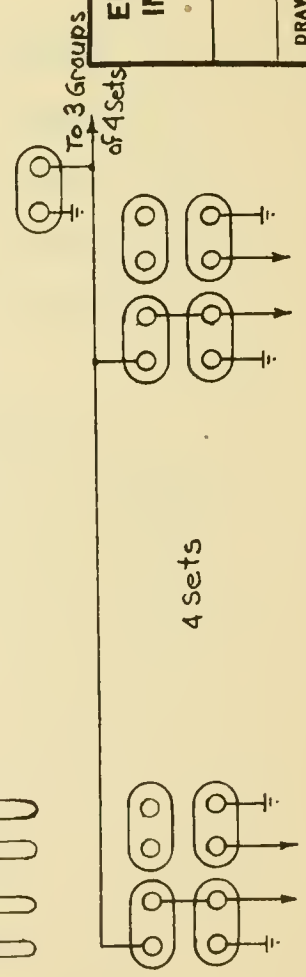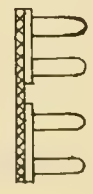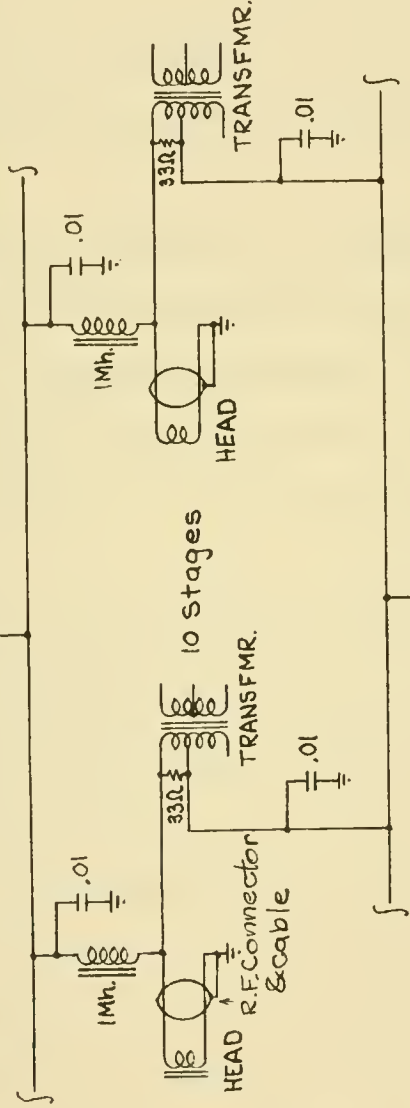
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INSTITUTE FOR ADVANCED STUDY
PRINCETON. N.J.

DRUM ERASE

DRAWN: F. Fell   DATE: 1-13-56

SCALE: Dwg. No. A-2568

The transformer secondaries are incapable of maintaining the sustained 60 ~ current required for erasure since their low impedance to 60 ~ would imply excessively large currents for sufficient head current. It was necessary therefore to disconnect the secondary during erasure. Since it was desired to erase groups of ten tracks simultaneously, provision had to be made for common connections which would insure adequate decoupling between each of the ten transformers during normal read and write operations.

A common secondary return bus is normally plugged to ground. A capacitor to ground at each transformer return eliminates crosstalk in that bus during read and write sequences. Removal of the ground lifts the transformer returns from effective 60 ~ ground thus preventing erase current of any significant magnitude from flowing in the transformer windings.

The upper end of each transformer secondary is connected to a common erase line through a filter which is effective at the frequencies involved in reading and writing. (The smallest frequency is that of a single sine wave of period 8 μs., so f = 125 K.C.) Since the erase line is grounded by a plug arrangement for normal operation, the individual transformers are effectively isolated from each other. During erase the erase bus is connected to the 60 ~ source and since the reactance of the filters is now negligible, the erase current will flow into the ten heads in the group and bring the desired tracks to an unmagnetized state.

The necessity for drum erasure is infrequent and is generally a servicing procedure if writing should ever occur inadvertently between the normally designated sync spaces, or if greater than normal writing

current should ever occur, applying "spread-out" signals to the drum surface.

10) θ and track counters - Dwg. #0-2565.
    Interlace counter - Dwg. #0-2558.

The θ counter is a 12 stage half-adder counter which is reset to zero with each drum revolution ("O" pulse time) and which is gated by the "S" pulse and utilizes 'S' for its carry input. Logical details of this counter are found in section c.i and c.ii.

The two stage track counter, part of the θ chassis, is of the same basic form as the θ counter (as is the three stage interlace counter). It is gated by set-up initially. Thereafter a gate is produced by the "O" pulse when recognition is achieved and a count of 111 is in the interlace counter. The absence of these signals produces a carry in.

The reasons for these conditions may be seen by reference to the basic drum timing chart. Note that the number designations for θ are sequential, and refer to the absolute count of sync pulses as seen by the θ counter. The number designations for Rec. (Recognition) are the actual addresses called for by the coder, and appear in the order shown due to the 8 to 1 interlace. Consider now the one singular case where 4095 happened to be the first address referred to. Recognition has occurred, and an "O" pulse is the next sync pulse to come up. Since 4095 is the last address in a group or track (4096 words around the drum, and the group is 0-4095), track count advance must be made. The interlace counter was primed with a full 111 count at set-up time and cannot have changed since no "S" pulses came after recognition for this case. (See
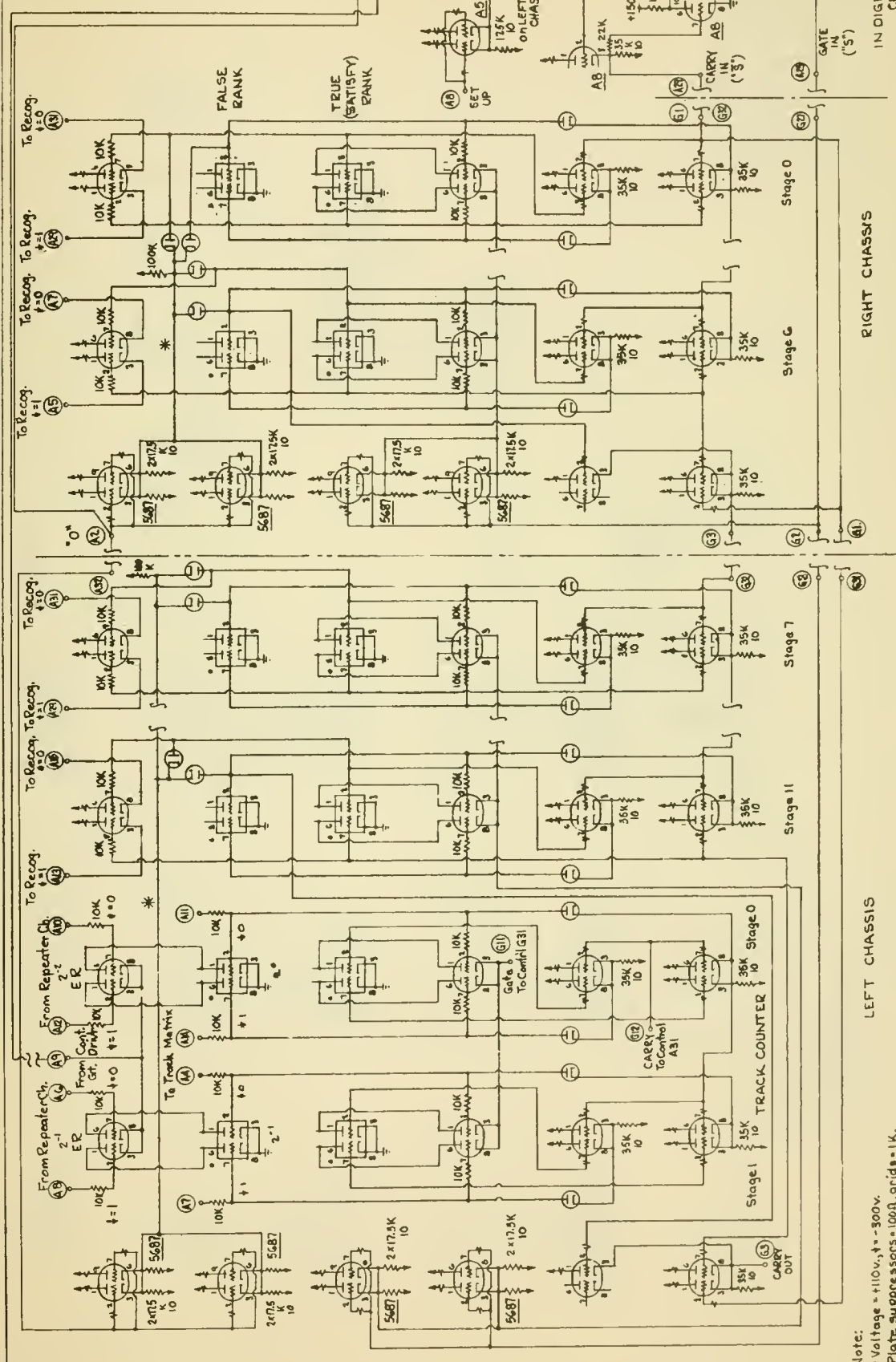
THETA & TRACK C.T.R.

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Note:
† Voltage = +110v, ‡ = -300v.
* Plate suppressors = 100Ω, grids = 1K.
Tubes are 5965 exc. as noted.
Diodes are Hughes 1N117.

* Clear all toggles but 0 is FALSE
to zero at "0" pulse time.

LEFT CHASSIS

RIGHT CHASSIS

IN DIGIT REPEATER CHASSIS

ON RIGHT CONTROL CHASSIS

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DRUM INTERLACE COUNTER &
EXCLUSION CIRCUIT

DRWN F.Fell   DATE 12-20-55

DWG. No. 0-2558
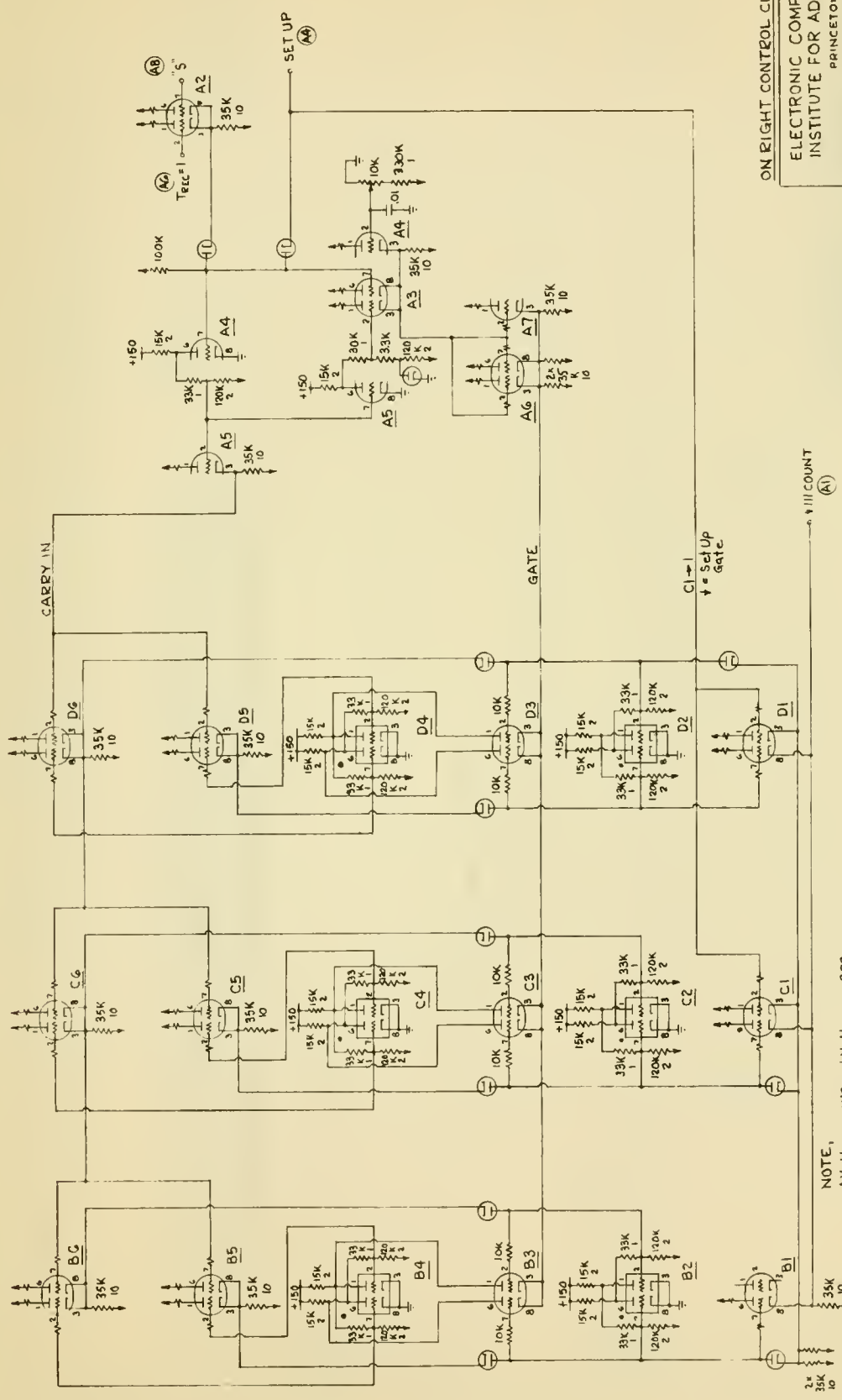
NOTE:
↑ Voltage = +110v, ↓ Voltage = -300
Plate suppressors are 100Ω ¼ w.; Grids are 1K, ½ w.
Tubes are 5965
Diodes are Hughes 1N117.
Located on Right Control Chassis
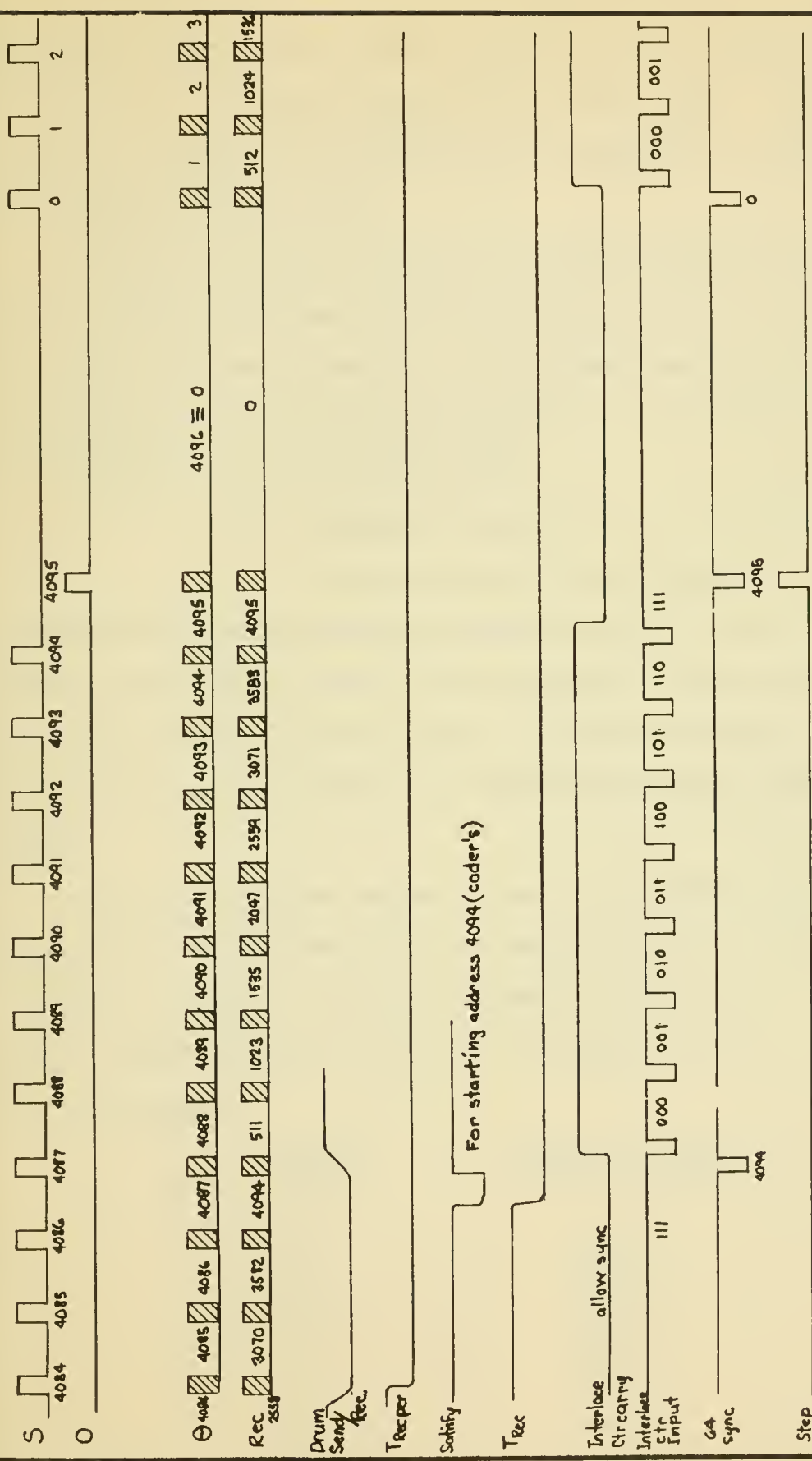
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BASIC DRUM TIMING

DRAWN: F. Fell   DATE: 6-26-56

SCALE: Dwg. No. A-2580

Drum Timing Control, section c.ii.) The "0" pulse now completes the conditions for a stepping operation on the track counter. Hence as the origin gap is passed a new track will be in readiness for operation with the resumption of sync pulses.

For all other cases but the one singularity mentioned above, the interlace counter will have been advanced after recognition. Examination of the sequences for any such case will show that a new track is selected at an "0" pulse time coincident with a 111 interlace count which can occur only at a count of 4095.

11) Coincidence recognition - Dwg. #A-2560.

This circuit has the simple function of inspecting for equality between the requested starting address presented by ER and the address residing in the θ counter. Only when these two numbers are identical, digit for digit, will the θ satisfy bus be allowed to go to -30 v. (from ≈ + 5) and produce a unique recognition signal.

Since the interlace imposes a count on the surface of the drum which differs from the monotonic count provided by the θ counter, provision must be made for obtaining agreement between ER and θ, i.e. making θ count virtually in steps of 8. Beginning after the origin gap the counts must be:

θ Count	Recognition Count
0	0
1	512
2	1024
3	1536
4	2048
5	2560
6	3072
7	3584
8	1
9	513
etc.	etc.

TUBES	θ DIGIT No.	TERMINALS			ER₂ DIGIT No.
		θ₀	θ₁	ER₁	
E1,2	6	G7	G6	G2	2^{11}
F1,2	5	G8	G5	G4	2^{12}
E3,4	4	G15	G14	G10	2^{13}
F3,4	3	G16	G13	G12	2^{14}
E5,6	2	G23	G22	G18	2^{3}
F5,6	1	G24	G21	G20	2^{4}
F7,8	0	G32	G29	G28	2^{5}
E1,2	11	G7	G6	G2	2^{6}
F1,2	10	G8	G5	G4	2^{7}
F3,4	9	G16	G13	G12	2^{8}
F5,6	8	G24	G21	G20	2^{9}
F7,8	7	G32	G29	G28	2^{10}

RIGHT

LEFT

Terminal Strips

Terminal Columns

A ... G

LEFT CHASSIS

Tube Columns

2^6 2^7 2^8 2^9 2^{10}

RIGHT CHASSIS

2^{11} 2^{12} 2^{13} 2^{14} 2^3 2^4 2^5

↓=0 Tube Rows

ER ↓=1

ΘSAT. Bus

ΘCTR. ↓=0

ΘCTR ↓=1

RECOGNITION

LEFT Θ CHASSIS

RECOGNITION

RIGHT Θ CHASSIS

This relationship is accomplished by a simple perversion of digit lines feeding the recognition circuit and is shown below:
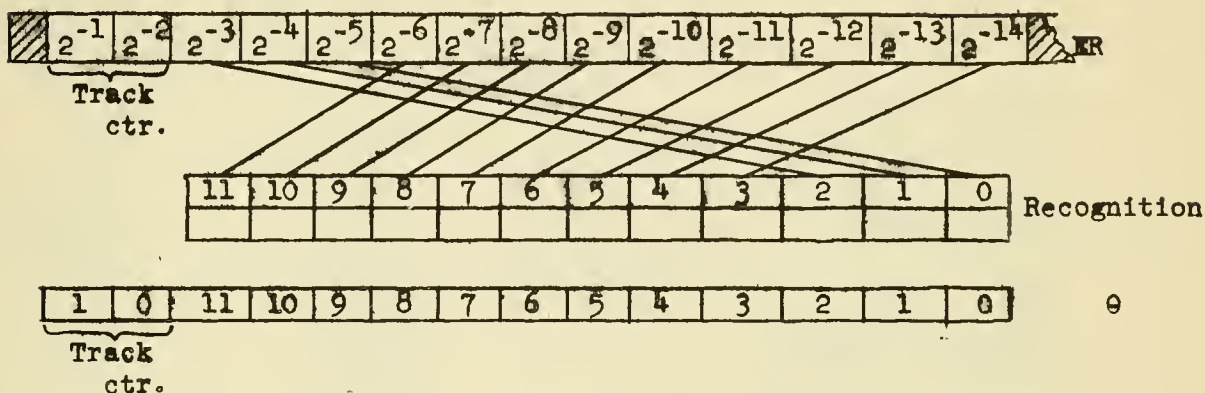
12) Control - Dwg. #0-2557.

This control circuit is a direct electronic realization of the logical flow previously described. All logical elements are the same as those in standard use at this laboratory.

d. Physical realization and operation experience.

1. Construction.

Initial planning for the drum and external devices was begun in February 1955. Construction was begun by June of that year and completed on schedule by 1 February of this year.

The external cabinet consists of two bays of enclosed cabinets, each 6' x 2' x 2', and the drum cabinet comprises three bays of the same size. Most of the construction employed the miniature tube curved chassis in general use at this project. A total of about 1000 tubes and 200 germanium diodes were required. Cooling is accomplished by multiple blowers in the cabinet bases. All interconnections and external cablint was done with shielded AN connectors. The only shielded wiring requirement was that for the drum amplifier outputs to minimize crosstalk.

DRUM CONTROL

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DRWN FF41
DATE 12-16-55
DwgNo. D-2557
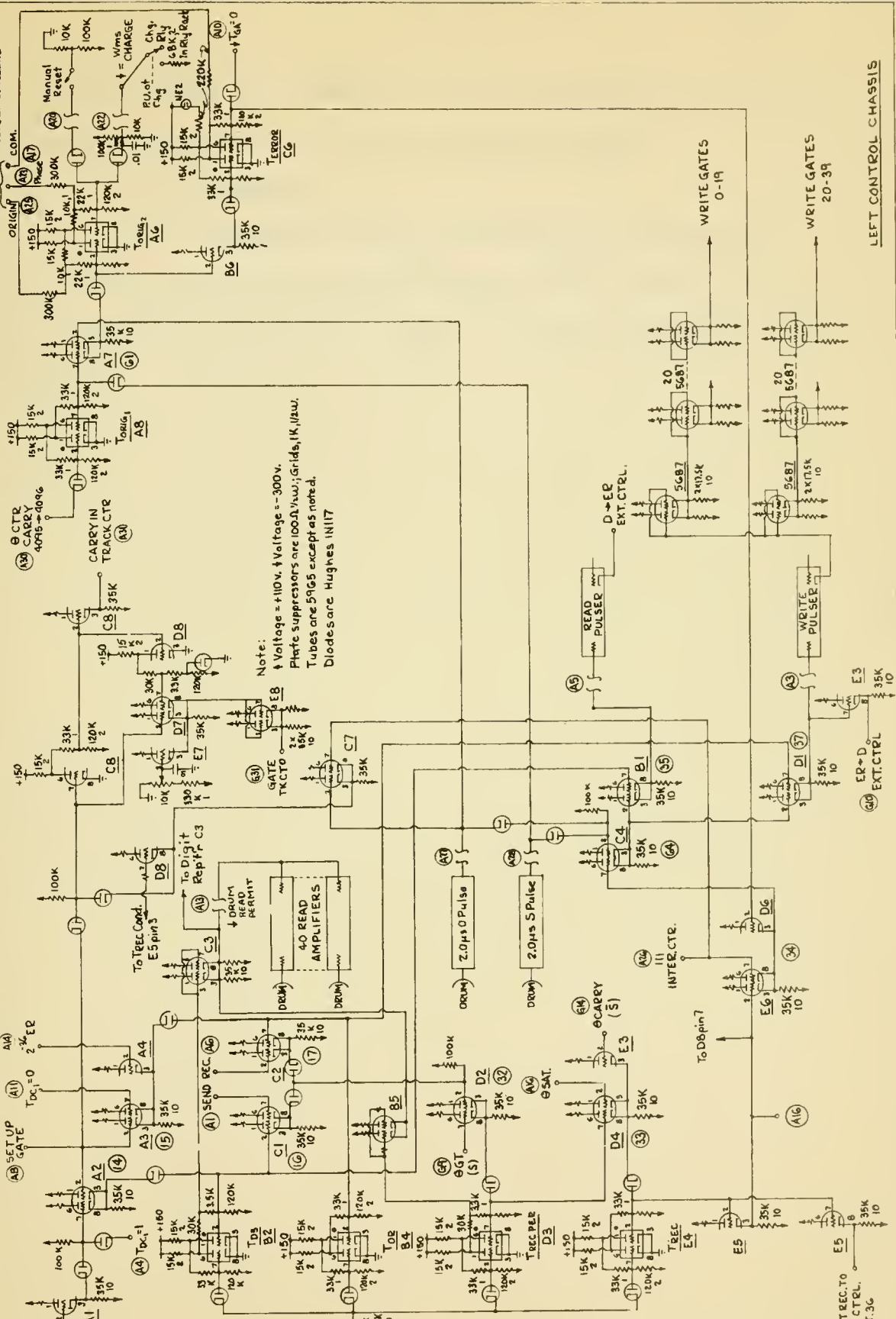
Note:
↑Voltage = +110v. ↓Voltage = −300v.
Plate suppressors are 100Ω/vw.; Grids, 1K, 1/2w.
Tubes are 5965 except as noted.
Diodes are Hughes 1N117

LEFT CONTROL CHASSIS

WRITE GATES 0-19

WRITE GATES 20-39

Filament turnon is accomplished by local variacs, and B+ turnon and turnoff is sequenced by the existing machine circuits.

ii. Operation.

Preliminary testing and debugging operations were begun in February 1956 and all tests concluded in June. This period included an exhaustive rundown of all phases of operation, including marginal testing.

2. Experimental Work.

    a. Introduction.

        A substantial portion of the engineering effort during the period of this report was directed to the design and construction of the new input-output system. However, other work was done, particularly in the direction of higher speed circuitry. Consideration was restricted to the case of a parallel asychronous machine with a word length of at least 40 binary digits. The problem was resolved into three broad lines of attack: (1) speed-up of parallel arithmetic unit information transfers (2) speed-up of serial information transfers and (3) speed up of the inner memory. Item (3) is of course a special case of (1) but of such great importance as to warrant separate consideration.

        A limited amount of work was done on items (1) and (3) and this is reported below in section 2.b. A reasonably good solution of (2) was accomplished and is reported in section 2.c. The essence of section c. has also been assured as a separate report and paper. Some work was done on larger Williams memories and is reported in section d. The conclusions of this effort were mainly negative. Finally the rather unique chassis construction employed at this project is described in section e.

    b. Speed-up of parallel information transfers.

        A parallel information transfer consists of transmitting information held in one set of toggles through a set of gates into another set of toggles. Such a transfer is viewed as starting when the set of gates are first enabled and ending when the receiving set of toggles are themselves able to transmit their new information elsewhere.

The total time taken by a transfer is therefore a function of the toggle-gate complex, not of the toggle or the gate alone.

At the present time these toggle-gate complexes could be made with either vacuum tube or transistor circuitry. Since the speed of transistor circuits depends so much on the type of transistor used, no study of them is planned until some of the recent fast units can be obtained. A modest study of vacuum tube circuits seemed desirable if only to define their limits and perhaps sharpen the competition with transistors. Because this study showed that even some presently available transistors, notably the Philco SB-100, exceed vacuum tube speeds only the most promising vacuum tube circuit will be described.

The fastest vacuum tube toggle-gate complex worked on is shown below:
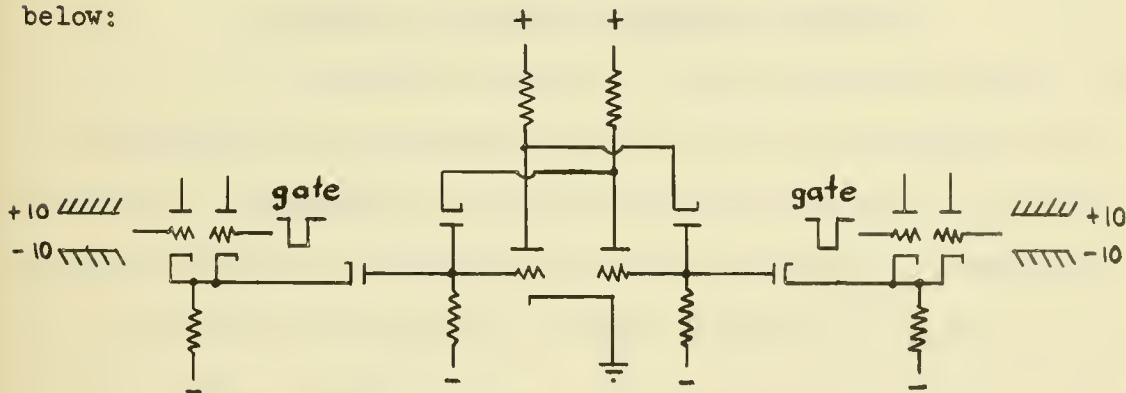
The usual plate-to-grid transpose resistors have been replaced by silicon junction diodes connected in reverse and biased to the breakdown state. They function essentially as batteries to transmit the plate signal to the grid without attenuation or delay. Diodes with 30 to 40 volt breakdown would be desirable; the circuit was tried with 60

volt diodes which were available but led to larger voltage swings than needed. The complete transfer time was in the range 0.08 to 0.10 microseconds.

As noted before, the inner memory is a special case of parallel information transfers. A memory reasonably consistent with the above toggle-gate speeds and with the carry speed reported in section c. should have a total cycle time of not more than 1 microsecond. A lower limit for the present type of Williams memory appears to be about 3 microseconds, to go shorter one must sacrifice an already small signal output. A workable electrostatic memory in the microsecond range should be possible using the Radechon tube (RCA 6499). One of these tubes has been procured but no significant work done with it as yet.

c. Speed-up of serial information transfers.

A very basic feature of the IAS machine is that it is not clock-controlled (except the memory unit) but rather operates asynchronously. Essentially this means that time is not quantized. The machine is viewed as performing elementary operations, one after the other, with each such operation having the property of beginning at a "start" command, running as long as needed, and upon finishing emitting a "finished" signal. Each "finished" signal from a previous operation is used as the "start" signal for the next. The "finished" signal may be derived with varying degrees of rigor. Ideally it should mean that exactly the operation called for has been done and done correctly. For example, the operation of gating is generally intended to impress the number pattern in one set of toggles upon a second set, and the gate command should be held on until and if equality is obtained between the

two sets. The equipment needed for sensing equality can be quite ex-
pensive. As a practical matter one may have to settle for something
less than this. For example gate pulse durations in the present machine
are determined by inspecting for the successful and complete flip of a
prototype toggle in the control. Here the one toggle stands as an
analog for the behavior of 40.

An important advantage claimed for the asynchronous mode of opera-
tion is just that the time taken by an elementary operation is irrelevant
except in determining the overall machine speed. This allows great
flexibility in the overall design both in tailoring the specific set of
operations to an individual user's need and in permitting engineering
changes in one of a set without disturbing the time relations with the
others. In particular one may take advantage of the average properties
of the elementary machine operations, combinations of which form the
basic arithmetic and logical processes. The essentially serial carry
process arising in the parallel addition of numbers is one such ele-
mentary operation. A method is given for significantly decreasing the
time required for the carry process by using the average properties of
carry sequences. Such a method is of particular interest not just for
the addition operation itself, but also for the possibility of speeding
up the ordinary repeated addition type of multiplication, since it would
be of great value if this simple type of multiplication could be per-
formed in a time comparable with the potentially fast but equipmentwise
expensive simultaneous multiplication.

We distinguish the carry propagation, which is serial, from the
formation of the sum digit, which is parallel given the carries. Thus

assuming the addends to be applied simultaneously to the N parallel stages of the adder at time t_0, we observe the carry into the most significant stage of the adder and call the time t_1 when it recognizably assumes its final value. We define the N stage carry time to be NC = t_1 - t_0 when the carry arises at the least significant stage and progresses through to the most significant. At least a majority of existing machines employ carry circuits in which the full length carry time NC must necessarily be allowed in each addition. The required time allowance is typically provided by a separate timing device such as a multivibrator so that the actual time provided must be NC plus a safety margin to allow for tolerances in both the carry circuit and the timing device.

In practice this safety margin may be an appreciable fraction of NC. Every designer of an asynchronous machine has probably considered using the carry circuit to time its own full length carry time NC. One such method is given by Richards[1] and a similar method is also embodied in the logic to be described. These methods certainly increase the timing reliability of the carry system and also save the above mentioned safety margin.

A more significant speed-up can be made if time is allowed only for the actual carries arising in the particular additions. In an early discussion of the logical design of a computer[2] it was shown that on the average the maximum length of a 1's carry sequence in a 40 digit addi-

---

[1] R. K. Richards, Arithmetic Operations in Digital Computers, Van Nostrand, 1955, pp. 138-140.

[2] Burks, Goldstine, and von Neumann, Preliminary Discussion of the Logical Design of an Electronic Computing Instrument, 1947.

tion is only 4.6 stages. If fully exploited, this result could lead to an 8 fold saving in average carry time. Such a saving, resulting from logic alone, has the important property of being additional to that resulting from faster components. The logic to be described gives almost this 8 fold saving. It differs from the optimum in that carry sequences of 0's as well as 1's must be considered and in this case the average maximum carry sequence is shown to be 5.6 stages.

C_{in}	A	B	C_{out}	
0	0	1	0	
0	1	0	0	carry out is determined by carry in
1	0	1	1	
1	1	0	1	
0	0	0	0	
1	0	0	0	carry out is determined solely by the
0	1	1	1	addends A, B
1	1	1	1	

Figure 1.

Figure 1 shows the truth table for determining the output carry, C_{out}, for one stage of a binary adder, the inputs to which are the addends A and B and the input carry C_{in}. The eight input combinations are divided into two groups of four each according to whether or not the output carry can be stated independently of the input carry. We establish our nomenclature by considering first the simple carry determination logic given in figure 2. Here the symbol $(\overline{00})$ means that not both A and

B are zero, while (11) means that both A and B are ones. C^1 indicates a carry of one.

This simple carry circuit is incapable of providing its own timing because of the carry interruptions (caused by 00) and carry starts (caused by 11) which may occur variously throughout the N stages. A symmetrical treatment involving also 0 carries (C^0) as in figure 3 results in a circuit which can provide its own timing. Essentially a separate carry chain is provided for the 1's and for the 0's. The state of the carry lines should now be viewed as "off" or "one" for C^1 and "off" or "zero" for C^0. At the beginning of an addition, both carry lines are "off". This condition will be met if both carry inputs to the least significant stage are held "off". The carry sequence is begun by setting one of these inputs, say C^0, to the "on" state. This carry will then proceed down the "0" chain until it reaches a stage having (11) at which stage the carry switches over to the "1" chain. Similarly it will then proceed down the 1 chain until it reaches a stage having (00) where it will switch back to the zero chain. Finally it will emerge from the most significant stage as either a C^0 or a C^1 to signal the end of the N stage carry. This zig-zag process is indicated schematically in the upper part of figure 4 which traces the carry chains through ten stages of an adder with the given addends A and B. It should be emphasized that the carry will always pass serially through ten stages although the route will be determined by the addends.

THE LOGICAL CIRCUIT

A re-examination of figure 1 in the light of this circuit leads to the logic for deriving a completion signal for the actual carries.
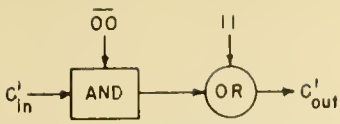
Figure 2   Simple carry logic.
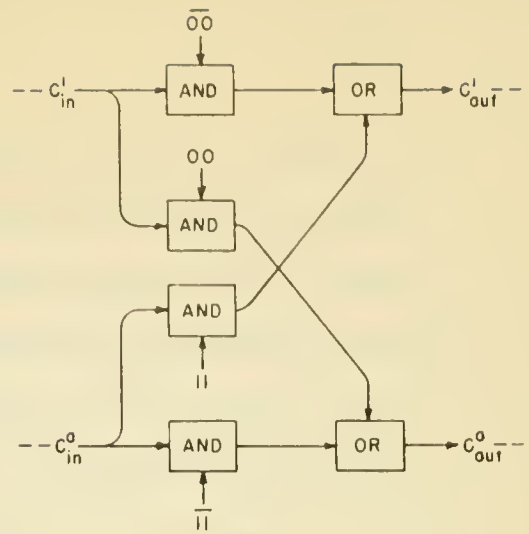
Figure 3   Logic for self-timing full length carry.
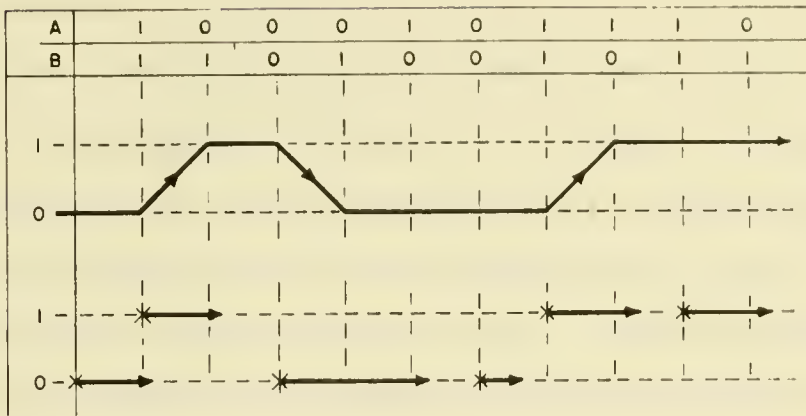
Figure 4   Carry sequences in ten consecutive adder stages with addends
            A and B. Upper sequence is for logic of figure 3 and lower
            sequence is for logic of figure 5.
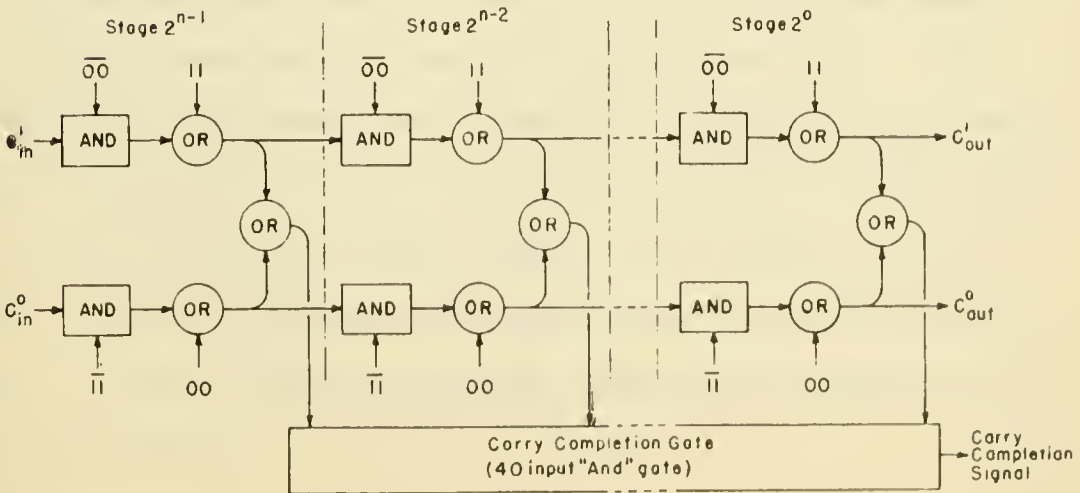
Figure 5   Logic for self-timing actual carries.

The first four cases are seen to be the ones for which the output carry depends on the input carry while in the latter four cases the output carry isindependent of the input. This result is made use of in the logic shown in figure 5. The dual carry chains of the previous circuit have been retained but the C_{in} restrictions on (11) and (00), that is the cross connections, have been deleted. An N input "and" gate has been added to signal the presence of a carry (1 or 0) at each of the 40 stages. As before, both carry lines are off at the start of an addition, this being enforced for the interior stages by an explicit parallel inhibition on the lines or by operating on the 11 and 00 inputs. Carries are begun by releasing the inhibitions on all stages, including the selected carry into the least significant stage. At this moment carry sequences will arise not only from the selected input carry but also from every interior stage having (00) or (11). Thus the serial aspect of the carry is restricted to sequences of stages for which A ≠ B.

The lower half of figure 4 shows the carry chains resulting for this final circuit using the same addends as previously. Six carry sequences are started simultaneously as marked by the asterisks. Since for the so-marked stages the input carry is irrelevant to the output carry, incoming carry sequences stop at the stage just prior. Now it is seen that for this example the longest carry sequence is three stages instead of the full ten. For the more practical case of 40 digit numbers it is shown below that the average longest carry sequence will be 5.6 stages. Thus after an average time delay of only 5.6 C each of the 40 inputs to the carry completion gate will be enabled, signalling the end of the carry process.

PROPERTIES OF CARRY SEQUENCES

The analytic approach of Burks et al (loc. cit.) to the problem
of determining the properties of 1's carry sequences is unable to give
more than the value of the average maximum carry sequence and gives no
information as to the variance of this maximum carry. Thus, while in
principle we could have extended this analytic approach to include the
present case of both 0 and 1's carry sequences, it was decided to obtain
the results by actual numerical experiment so as to gain some knowledge
as to the variance.

A code was therefore written for the IAS computer to examine the
properties of carry sequences. This code generates pairs of random 40
digit numbers and adds them digit by digit so as to obtain for each
pair of numbers the maximum carry sequence (n max) of 1's or 0's arising.
The distribution of n max found from 4000 random additions is shown in
figure 6. The distribution was unchanged by increasing the sample size.
From these results the average maximum carry length, defined as
$\sum_{n\ max} P(n_{max}) \cdot n_{max}$ was found to be 5.6. It is of interest to note the
small deviation of the individual maximum carry length from this average.
This is brought out by figure 7 which shows the percentage of additions
which have a maximum carry sequence greater than n.

It seemed desirable also to check the carry sequence properties
of the interior additions involved in the simple multiplication process
mentioned earlier. Using a similar code to that for examining addition
it was found that again the average maximum carry length was 5.6. Thus
in a typical multiplication of two forty-digit numbers the average sum
of the individual maximum carries will be 20 x 5.6 = 112.
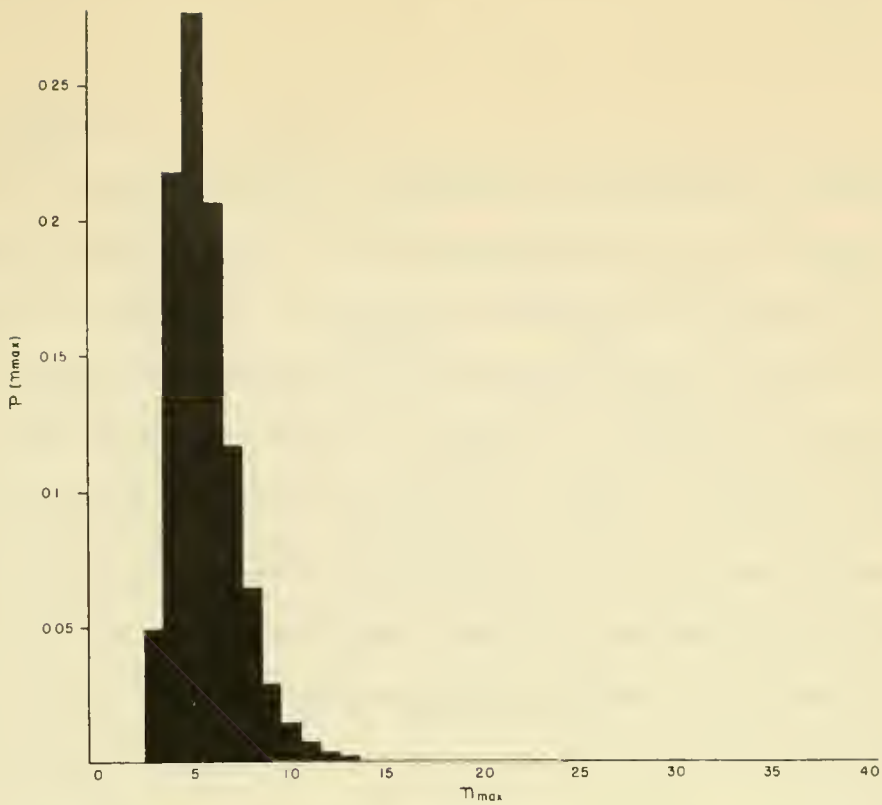
Figure 6 Probability distribution of the maximum length carry sequence (n_{max}) arising in a forty digit addition.
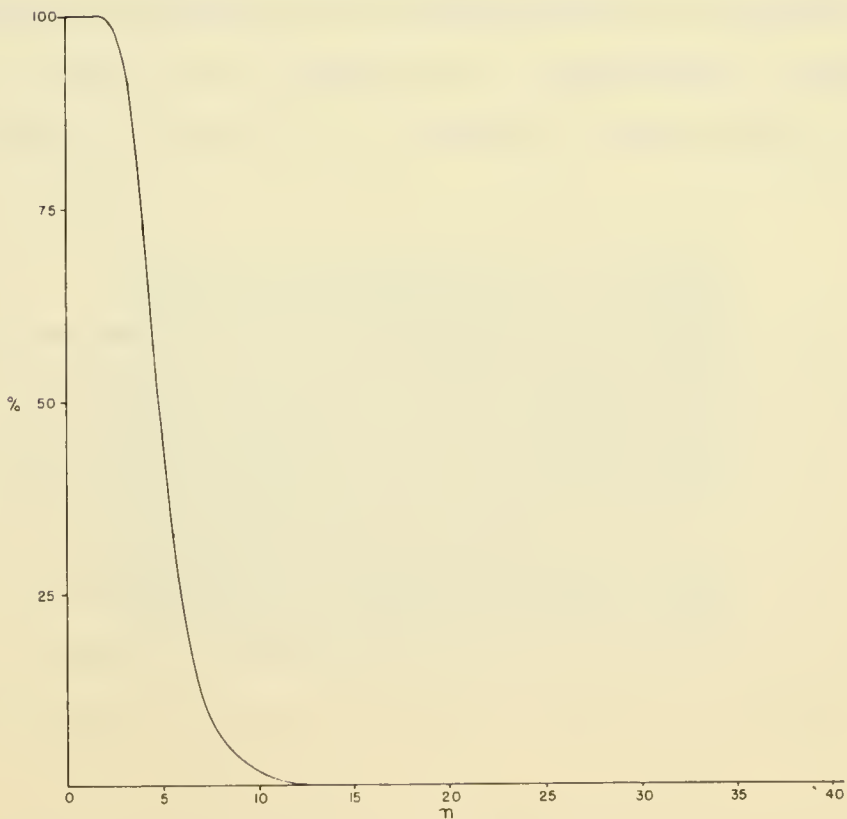
Figure 7 Percentage of additions having a maximum length carry sequence greater than n.

EXPERIMENTAL RESULTS

An eight stage experimental accumulator was constructed embodying the carry logic described above. The per-stage circuit for the carry portion is shown in figure 8. It should be noted that the digit logic, registers, and gates were connected to this carry circuit in order to present the loads which would obtain in actual use. Figure 9 shows the response of this circuit to carry sequences of several different lengths. In each case carries were started by enabling the carry lines and the carry input C^o to the least significant stage and observations were made at the output of the 8 input "and" gate. The leftmost curve shows the carry start signal and successive curves to the right show the completion signals for carry sequences of lengths 0, 2, 4, 6, and 8, respectively, completion being represented by a negative going signal. We define the moment of completion as the time at which the signal passes below -5 volts. Of particular interest are the times required for the carries of length 4 and 6, which are 0.18 µs and 0.22 µs, respectively. Hence the average carry time per addition will lie between 0.18 and 0.22 µs, or approximately 0.21 µs.

CONSLUSIONS

A method has been shown for accomplishing the carries of a 40 digit addition in an average time of 0.21 µs by using a self-timed carry logic. Preliminary results indicate that the remaining essentially parallel portion of the addition can be performed in about 0.15 µs. If this figure can be maintained, the average total time, exclusive of memory access, required for an addition could be 0.36 µs and that for a multiplication could be 40 x 0.15 + 20 x 0.21 = 10.2 µs. The carry
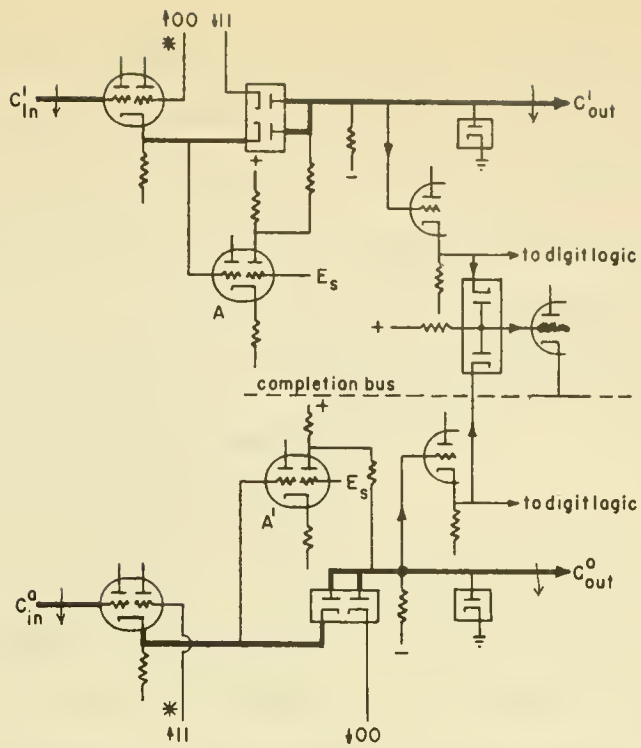
* parallel carry turn-off also
$E_s \approx -5$ volts. Tubes A & A' restandardize carry as needed.

Figure 8   Per-stage carry circuit of experimental adder.
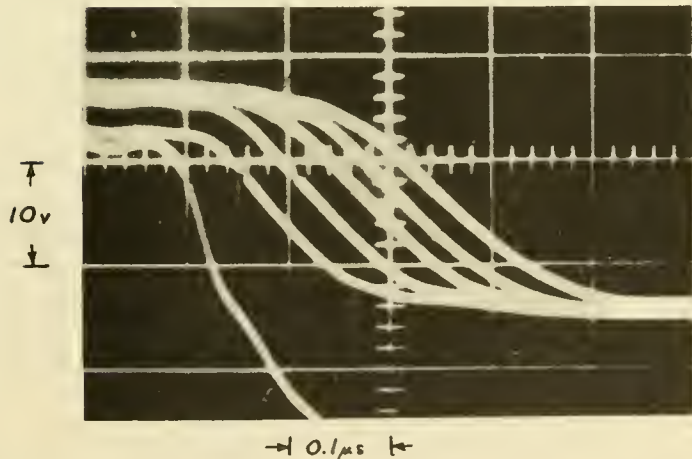
Figure 9   Completion signals for several carry lengths in eight stage
experimental adder.

circuit used requires more components than those in generally used carry circuits, but offsetting the increased complexity is the significant increase in speed. In addition, the inclusion of the 40 stage "and" gate permits a carry-less determination of the equality of two addends, this mode being obtained by not releasing the parallel carry inhibitions shown in figure 8. In this case an output is obtained from the carry completion gate if and only if the two addends are equal.

A NOTE ON HIGH SPEED DIGITAL MULTIPLICATION

In a recent paper Gilchrist, Pomerene and Wong[1] (GPW) showed how the carry logic of a digital computer could be arranged so as to make use of the theoretical result that the average carry sequence arising in the addition of two binary numbers is considerably less than the length of the numbers being added. In the concluding paragraph of this paper the authors made an estimate of the expected time for a multiplication using such circuitry. It is with reference to this estimate that this note is written.

Burks et al. (loc. cit.) noted that if multiplication is carried out by successive additions it is sufficient to allow but a single carry at each intermediate stage and that a complete set of carries is needed at the end only. The question immediately arises as to whether this final set of carries obeys the same statistical properties as those formed in the addition of two random numbers. To verify that this is the case the numerical experiments described by GPW were repeated with the modification that only one carry was allowed at each intermediate

---

[1] Fast carry logic for digital computers. I.R.E. Trans., vol. EC4, pp. 133-136, Dec. 1955.

stage of the multiplication and the average length of the final complete

carry determined.   This was found to be 5.6 for the multiplication of

two 40 digit numbers and the probability distribution of the maximum

carry sequence was found to be the same as that for simple addition

given in figure 6 of GPW.

The actual sequence of operations involved in performing such

arithmetic is indicated in the logical diagram of figure 10 which shows
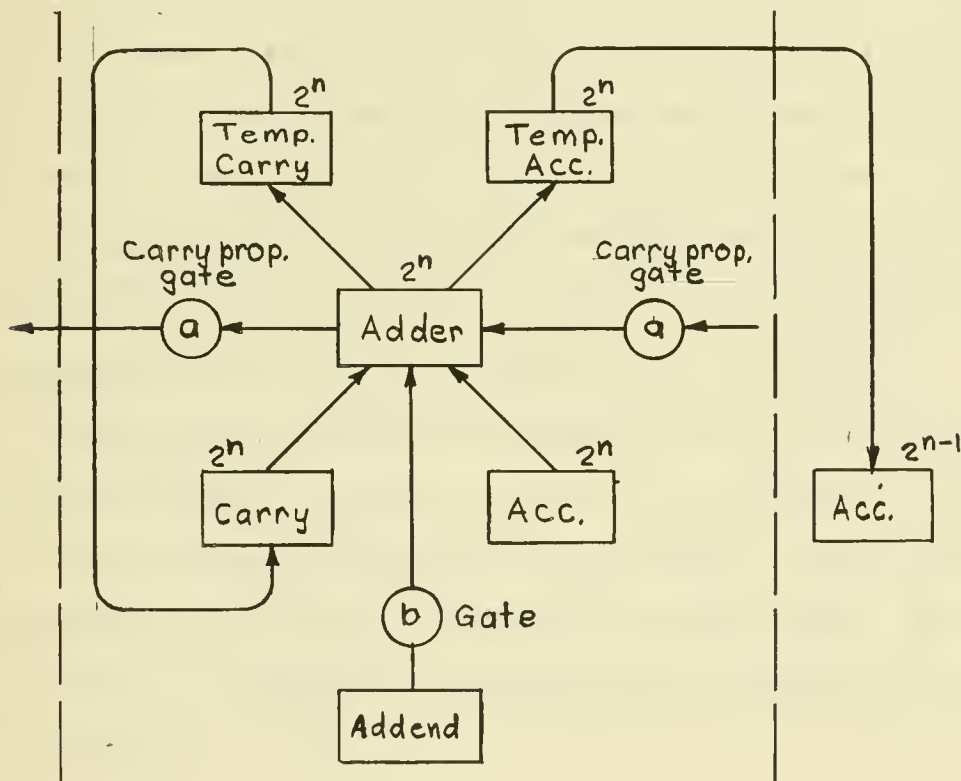
Figure 10

Legend for Figure 10.

Logical layout of the n'th stage of the parallel arithmetic organ.
The gates (a) are inhibited during all interior operations and enabled
for the final operation.   The gate (b) is enabled during all interior
operations and inhibited for the final operation.

an interior stage of the parallel arithmetic organ. At the beginning of
a multiplication operation the inputs to the n'th stage of the adder are
the n'th digits of the addend, the cleared accumulator and the carry
storage register. The sum of these quantities is held in the temporary
accumulator and the resulting carry is held in the temporary carry regis-
ter[1]. The contents of the temporary carry and accumulator registers are
then transferred into the permanent carry and accumulator registers.
This operation is repeated for each interior step of the multiplication
without, of course, clearing the addend and accumulator but with appro-
priate shifting of the accumulator. For the multiplication of two k
digit positive numbers there are k such interior operations. As a final
step the addend input is nullified and the carry propagation gates are
enabled with the circuitry described in GPW. A carry completion signal
is then produced and the final sum placed in the accumulator[2].

Utilizing the operation times given in GPW and the fact that the
average carry length in the last carry is 5.6, we obtain 41 x 0.15 + 0.26 =
6.4 us as the average multiplication time exclusive of memory access.
This compares with 10.2 us in the case of no carry storage. The cost of
this speed-up is an additional register for carry storage and associated
gating elements.

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[1] These temporary storage registers may be actual toggles or delays.

[2] If the numbers are not both positive and only one set of complement
gates is used, there are usually correction factors which have to be
introduced in extra steps of the process. These should all be done
prior to the long carry.

d. **High density Williams storage.**

Introduction. One great drawback of the Williams storage system is the read-around, or redistribution, trouble when used as a random access memory. It is well known that read-around can be improved by increasing the spacing between bits. In view of this fact, it can also be argued that if read-around can be restricted by using special modes of operation, packing can be increased. The inquiries were divided into roughly the following lines:

1) Most operating Williams storage systems assign two neighboring locations to store one bit of information. These locations each occupy about one spot diameter of the beam. If only one position was bombarded, this position will contain a positive charge due to the release of more secondary electrons than primary electrons arriving. If the two positions are bombarded in succession, then the first position will be charged negative due to the deposition of secondary electrons when the second position is bombarded. Thus two kinds of signals can be stored in the first position. The second position really does not store any information. If this second position can be shared between two neighboring bits, some improvement in packing should result.

2) The read-around and packing density trade is investigated by using the techniques of an operating Williams memory. The packing is increased until the Williams tube fails to store a prescribed sequence of ones and zeros.

3) The geometry of the cathode ray tube is also briefly investi-

gated. For a given size beam spot diameter, obviously the
larger the screen size, more will be the number of bits that
can be stored on a single Williams tube. Experiments were
carried out by using different sizes of cathode ray tubes.

4) Long term stability was not included in the investigations
    because this calls for significantly more elaborate equip-
    ment. Most experiments described in this paper were done on
    an exploratory basis and used a minimum amount of equipment,
    their details are therefore omitted.

It was envisioned that with increased packing, and employed in a
role similar to the magnetic drum, the Williams system should be more
flexible and may even be competitive in cost. An example of such usage
is provided by a hypothetical machine organization.

Experiments and results. Using the double-dot system and
circuitry similar to that in the IAS machine, it was found possible to
store successfully a mixed pattern of 64 x 64 on the 3" RCA C73621 cathode
ray tubes (believed to be the prototype of 6571 storage tube).

A mixed pattern is a random mixture of ones and zeros. This is
done by briefly introducing some noise into the system by mechanically
tapping the signal amplifier. Furthermore, the rasters can be shrunk to
occupy an area approximately 1.5" x 1.5". Five samples were tested and
are all capable of storing the mixed pattern, observed with a long per-
sistent oscilloscope with no visible change of the patterns over many
regeneration cycles.

Williams and Kilburn stated that a spot diameter is sufficient to
isolate neighboring bits. On this basis, a three-dot system is therefore

tried. Figure 1' shows a comparison between the two systems. The

shaded areas denote the positions at which the beam is turned on.

Clearly, the three-dot system may offer an increase of 50% or more in

packing.

A B   A B C
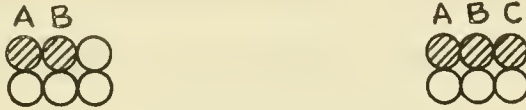
Figure 1'

Relative areas needed by the two-dot system
(left) and the three-dot system (right).

In the three-dot system, A and C each contain one bit of informa-

tion. The positions are inspected by turning the beam on at A and then

C, with their contents recorded in two flip-flops. Figure 2' shows the

amplied output signals through the four possible combinations. The con-

tents of A and C are destroyed after the inspection pulses. The beam is

0   0

1   1

1   0

0   1

A   C
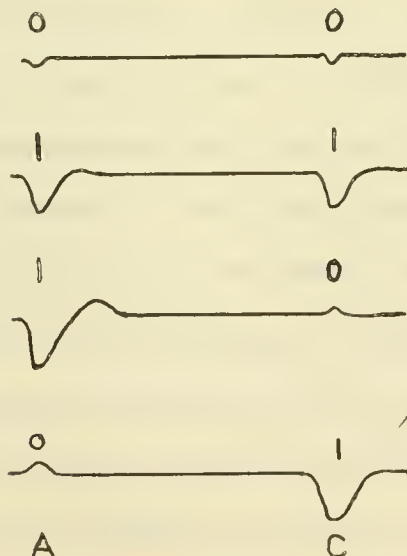
Figure 2'. Output signals with the 3-dot system.

then turned on at B to make both A and C to contain 1's. The beam is again turned on at position A to produce a zero at position A if A originally contains a zero and similarly for position C. For reasons of expediency, a 16 x 64 raster of this fashion successfully stores the four combinations of contents of A and C. There is room for two more such rasters on the face of the C73621 cathode-ray tube. Therefore it is believed that a 48 x 64 raster of this sort is possible.

The remaining series of experiments explores the packing density per tube by using various sizes of cathode ray tubes. Using the two-dot system throughout, one each of 5CP1A, 7VP1 and 17BP4A were tested. Both the 5CP1A and the 7VP1 can barely store the 64 x 64 raster when the rasters occupy the maximum permissible sizes. Since there is no obvious advantage to use the two types as far as packing is concerned, They are not considered any further.

A mixed pattern on a 16 x 128 raster was stored on a 17BP4A. This raster can be moved to store on different portions of the tube surface, with the necessary readjustment in focus. By careful manipulation, this raster can be made to occupy a space of 9/16" x 6" if it is placed in the center. By assuming each bit to occupy a space of six spot diameter squared, the spot diameter of the 17BP4A tested can be interpreted as approximately 1.7 times larger than that of the 3" storage tube. Obviously, the increase in screen diameter is many times that amount and therefore the increase in packing per tube should be greater with the 17BP4A or even larger tubes. Deflection defocusing of the big tube is quite severe, although methods of correction are straight-forward. Without focus correction, an attempt to store a 128 x 128 raster showed that

no one focus adjustment is satisfactory for the entire raster. This
point is not pursued further because the focus correction circuit is
external to the cathode ray tube and is not the subject of this in-
quiry.

To investigate the usefulness of a non-random access Williams
storage system, the following example is offered.
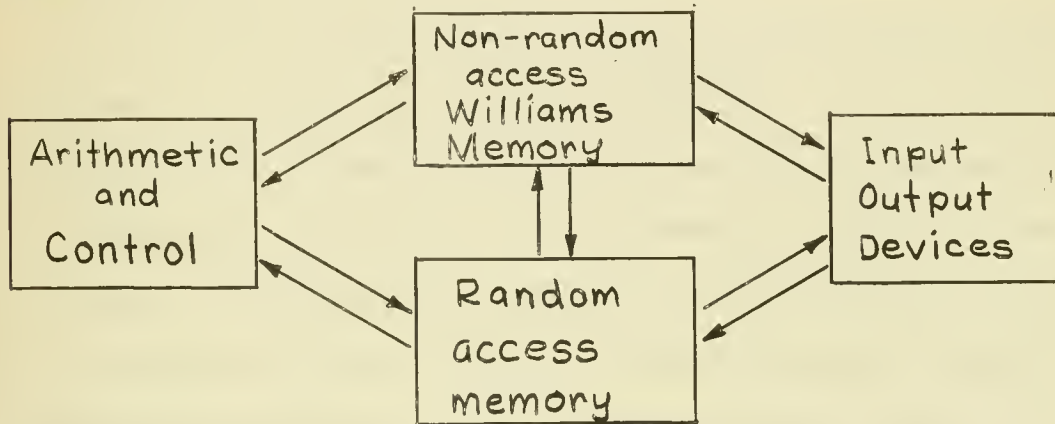
Figure 3'

An example of a machine organization using a non-random
access Williams Memory System.

It is necessary, of course, to have a random access memory for any
serious computation. The organization diagram of figure 3' indicates
that the non-random access Williams memory communicates with three
different units. Basically, the Williams memory regenerates its con-
tents in a sequential manner. It is intended that the information ex-
change between the Williams memory and the other three units be limited
to sufficiently long sequences. The faster the rate of occurrence, the
longer the sequences should be in order that regeneration can be in-
sured. Input-output units such as punched cards or tape have relatively
low slow rates. In these cases, it is only necessary to interrupt the

regeneration routine whenever a word is to be communicated between the Williams memory and the input-output devices. Most input-output routines consult the addresses of the Williams memory in sequence at a low slow rate, it is therefore possible to interlace the input-output routine with other routines imposed on the Williams memory without interference with each other.

If the communication between the Williams memory and the random-access memory is limited to blocks of information, it is practical to allow a jump in the regeneration routine to the starting address of the block. This then also becomes the new regeneration routine. A time delay equal to one regeneration cycle time is set in motion such that this time delay must expire before any further jump can be made, thus insuring a low read-around. This limitation actually is not too important if one recognizes the fact that usually after such a transfer, some time is devoted to arithmetic operations on the transferred words. Orders or data are quite often referred to in a sequential fashion. These references, however, usually occur at a much higher time rate and may equal or even exceed the speed of the Williams memory. It is permissible to interrupt but not alter the regeneration routine. A counter is needed to keep track of the work sequences. A similar time delay is set in motion so as to insure low read-around.

The foregoing example does show that Williams memory when operated in the manner described is more flexible than a magnetic drum. It is also possible to eliminate some of the access time normally unavoidable on the drum unless serious coding requirements are imposed.

Conclusion. A packing density of 4096 bits on a 3" storage

tube appears to be achievable without using radically different cir-
cuits. Access time can be reduced without impairing read-around by
suitable logical organization. The use of the three-dot system and the
use of television tubes as storage tubes must await developments in
circuitry in order to achieve reliability, but are certainly within the
realm of possibility.

    e. The design of standard chassis for experimental work.

    Rapid advances in printed circuit techniques and Tinker-
Toy type of waver assemblies have provided the electronic equipment manu-
facturer with a cheap and reliable means of producing repetitive cir-
cuits in large quantities. Unfortunately, no such panacea exists for
the equipment designer faced with the necessity of producing small
quantities of assemblies or families of units that can be basically
similar but must be individually flexible. This situation is particu-
larly true in the research and development field where the initial
cursory examination would seem to indicate that each assembly must be
special and unique.

    Obviosuly, the construction of chassis tailored to suit individual
circuits is a costly procedure; one that can produce sub and major assem-
blies that are neither functional nor aesthetic. In addition, the time
consumed in designing and producing such individual units is frequently
a source of minor irritation to the circuit engineer who naturally pre-
fers to test his ideas while the spirit moves him.

    In the interests of reducing costs and minimizing construction
time it behooves the equipment designer to examine the circuit require-
ments of the group that he services. While a perfunctory investigation
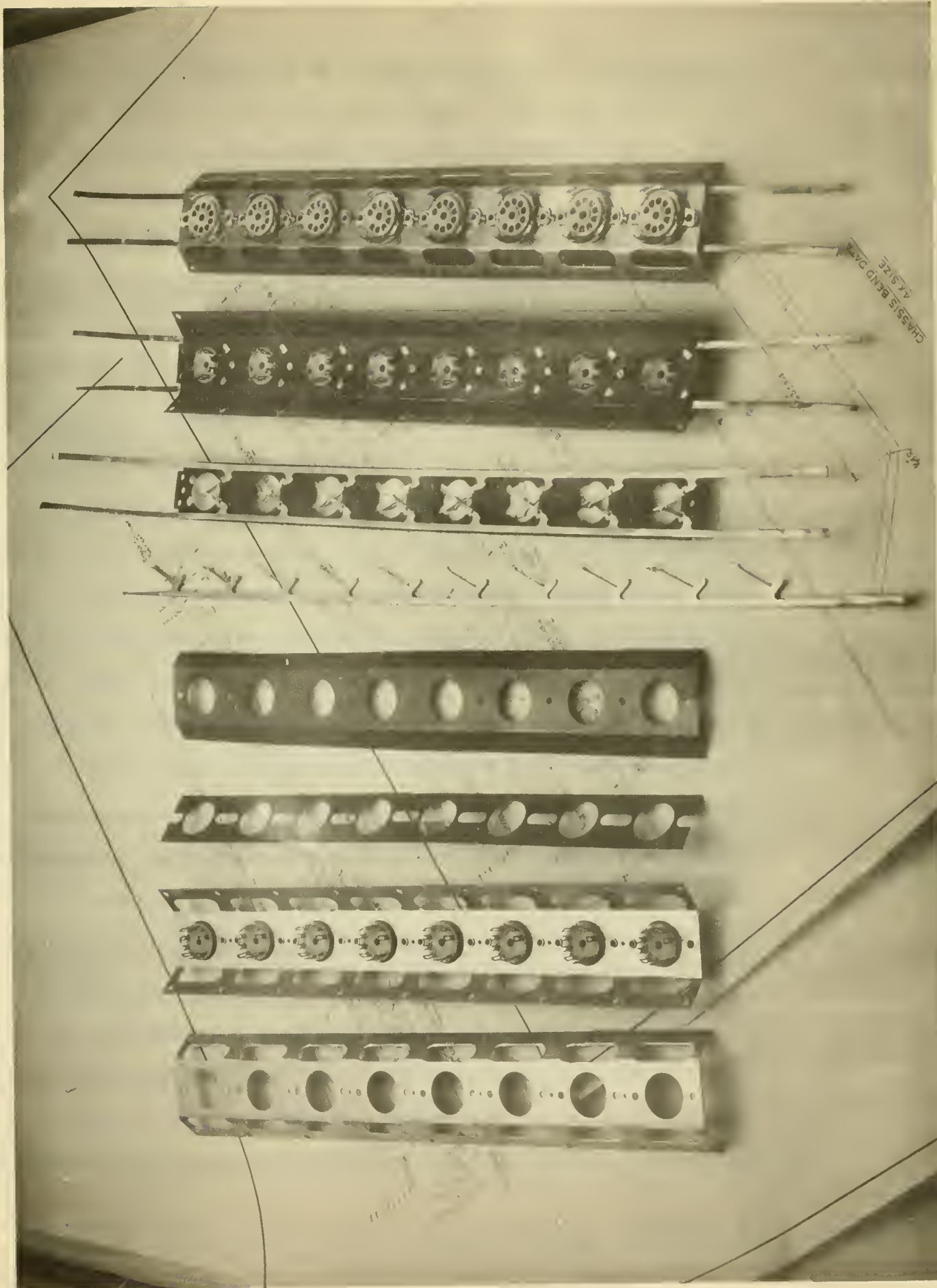
will reveal many parts capable of being standardized, a searching analysis may well pay off in the form of a standard, flexible, building block that can be manufactured economically in reasonable quantities, stocked as a shelf item and assembled like an Erector set.

The logical approach to designing an all purpose chassis is to enumerate the desirable characteristics as determined by the types of circuits and components involved. Having thus stated the problem, the solution becomes a matter of choosing the best possible alternatives to meet the stated conditions.

A somewhat statistical approach can be made by listing tube types and other standard components commonly used, the type of circuits normally dealt with and the usual means of intercommunication between stages and units. As an aid to establishing a standard, the possibility of physically separating the power supplies from the functional sections of the circuits should be considered. Elimination of such service functions will simplify the task of designing a basic unit.

The above points, viewed collectively, will most certainly emphasize those features and components that are common to the circuits under consideration. Delineation of the final unit then becomes a matter of designing a chassis around the standard components and techniques, providing for as much flexibility in the design as possible to accomodate special conditions.

The photograph illustrates a standard chassis, the individual parts of which are also pictured. Using these units as a basic chassis we have produced adders, registers, digit resolvers, pulsers, amplifiers and various control units incorporated in the IAS computer. They provide an

inexpensive and versatile basis for wiring experimental circuits in a minimum of time.

Our design and subsequent modification of the basic chasis was based on a variety of requirements. The nature of our research decreed that any standard chassis adopted be: Adaptable for serial, parallel and combined operation with other units; capable of accepting most, if not all, of the tube types commonly used in computer work; small; light; rugged; easily wired and serviced and capable of being produced in reasonable quantity without recourse to expensive equipment. Our wiring technique dictated that resistor leads be left a minimum of 3/8" long and that they be laid in place without bending leads wherever possible. Elimination of hookup wire, adequate ventilation and minimum intercommunication distances between adjacent tubes and units were given considerable weight.

Analysis of our program established the fact that 7 and 9 pin miniature tubes would be used in most of our circuit applications and any chassis accepting both sockets, in common and in combination, would satisfy this requirement. Composition resistors, mica and ceramic condensers and solid diodes emerged as supplementary components whose comparative size and application posed no real problems. This information completed the component picture and there remained only the determination of size and choice of shape. We chose to incorporate eight stages in the basic chassis since this number seemed to be a maximum as well as common size for us. A trapezoidal shape was chosen for a number of reasons; first, the semi-channel shape imparts rigidity to the unit, second, the shape lends itself to a curved assembly that vastly simplifies parallel

wiring and finally, we bought, at the price of a few well placed holes (in the main insulator), the ability to transfer some of the components to the upper side of the chassis thus relieving congestion around the tube socket; this without compromising our stipulation concerning resistor leads.

The chassis proper is formed from .032 aluminum alloy, 52S-1/2 Hard and the spacer and insulators are formed from nylon base bakelite. All of these parts were produced from dies made in our model shop and punched on a 4 ton punch press. An estimated 150 man hours of shop time were required to fabricate the entire set of dies.

Starting with an aluminum blank 2 5/16" wide by 12" long, eight 3/4" socket body holes are punched with one stroke of the press. The die that performs this operation contains eight punches staggered vertically so that no more than two punches are shearing the metal at any one time. This was done to avoid overloading the 4 ton press. A second die punches all of the socket mounting lug holes, center insulator mounting holes and edge holes in one pass. Oblong slots on either side are piloted on the 3/4" holes and punched progressively. They serve as clearance holes for resistor leads brought to the upper side of the chassis through holes in the main insulator. Forming to the trapezoidal shape is also done on the punch press.

Hugh H. Eby, Incorporated, makes a seven pin socket with the same mounting hole dimensions as their 9 pin socket. We found it quite practical to mount the 7 pin socket in the hole punched for a nine pin socket. The only objection to this procedure is the gap left between the 5/8" diameter socket body and the 3/4" diameter hole in the chassis

which, we felt, was a possible solder and dirt trap. The .016 bakelite spacer was designed to overcome this condition and to serve another function besides.

This spacer is punched in two variations, the first with eight 3/4" holes punched in the same die used to punch the metal chassis and the second with eight 5/8" holes. Both variations have the oblong slots which span and clear the two eyelets on adjacent sockets. The spacer then serves first as a shim to prevent the main and filament insulators from being distorted by the eyelet heads when they are drawn up against the metal chassis. In the assembly of a chassis with 7 pin sockets, the spacer with the 5/8" hole is used, not only as a shim but to close the gap between the 3/4" hole in the chassis and the smaller body of the socket. Where 7 and 9 pin sockets are mixed on one chassis, a hand operated punch can be used to enlarge the necessary number of 5/8" holes to 3/4" diameter in a minimum of time.

The main insulator is first punched to fit 9 pin socket bodies. In the second operation, seven .050" diameter holes are punched in the skirt on each side of every socket hole. When this part is bent and assembled each of these groups of holes centers in an oblong slot in the metal chassis. The holes are so located that a resistor lead can be wired from the upper side of the chassis directly to any tube pin without bending the lead. Folds in this .015" nylon bakelite part were post-formed in a crude aluminum die. Although nylon base bakelite is not normally regarded as a suitable post-forming material we experienced no difficulty with the thin sheet used. Ordinary soldering irons inserted in holes in the male and female die blocks provided sufficient heat to do

the forming.

This brings us to the filament bus strip and its insulator. The ladderlike shape of the copper strip comes from the press, and the finished strip with the excess metal is sheared off and round nosed clinching tabs bent for insertion into the insulator. A .015 x 7/8" continuous copper coil is fed into the die and blanked, one hole at a time, cut into 14" lengths and the excess trimmed on a shear. Unfortunately, we have as yet been unable to find a use for the unusual shaped slugs that are left. The bus strips are clinched to the insulator and easily connected to the socket pins. This completes the basic chassis, the parts of which are produced in quantities of 200 in a matter of three days.

This basic chassis can be tied to adjacent units by means of an aluminum angle tie strip to form an assembly of up to eight chassis. In any such assembly the Keystone shaped end bulkheads are eyeletted together where they overlap and, in addition to supporting cathode and plate busses, serve to stiffen the assembly. Initially, end bulkheads were fabricated in one piece, there being a different type of bulkhead for each type of assembly; viz: single dhassis bulkhead, two gang bulkhead, etc. This practice was inefficient for obvious reasons and additionally, four gang and larger units were difficult to assemble due to tolerance build-ups. The present end bulkhead is easy to make, economical of material and can be assembled easily, regardless of chassis bend tolerances.

During the past few years we have fabricated about 1000 of these basic units. Three other laboratories have built computers based on the

IAS computer and have used the same design successfully, not only in the machines but for experimental and breadboard circuitry. Although the basic unit does not serve all of our needs, its inherent versatility and flexibility have made it a popular item. In a matter of minutes a technician can draw the parts from stock, assemble them and begin wiring. This kind of utility is well worth the time spent in design and die making.

3. Machine Improvements.

a. Read around improvement.

In July 1954 the second anode voltage of the Williams memory cathode ray tubes was increased from 1000 volts to 1600 volts by changing the CRT cathode level from +300 to -300 volts. This change was presumed to put no greater stress on the heater wiring insulation. To make this change possible blocking condensers were installed in the CRT grid circuits so that the beam turn on pulse is no longer direct coupled. The "disconnect" diodes formerly used at this point were re-used as D.C. restorers. The third anode voltage was left unchanged at 2000 volts above cathode potential.

This change made it necessary to find completely new optimum settings for focus, astigmatism, and beam current for each CRT in the memory. In general the values of these parameters for best dot storage reliability (i.e. high read around) are not the same as for best dash storage reliability. The existing read around code served very well as a test of dot storage but up to this point dash storage could not be tested satisfactorily. An investigation showed that if a dash is stored and then read twice in succession before any neighboring points have been consulted, the second read out signal is about 10% smaller than normal. This situation would ordinarily not be programmed in a code but could happen as the sequence: store x, regenerate x, read x, in which case the dash signal may be marginal at read x time.

The discovery of this effect explained why dashes were occasionally lost in an apparently normal stage. A code was therefore written to pro- duce the above sequence at each point in the memory, always testing for

correct storage. This code proved to be the long desired dash relia-
bility test and was consequently entitled "Eureka". The use of "Eureka"
together with the read around code defines fairly well the state of the
memory and greatly helps in adjustment.

b. Extract order.

An "extract" or logical product order was added to the
machine in September 1954. This order is carried out in RII (i.e. the
quotient register) by withholding the clear $\longrightarrow$ 1 part of the normal
memory $\longrightarrow$ RII gating process. To see how this works, assume a word α
is in RII as a result of some previous order; the order $\beta \longrightarrow$ RII
(extract) combines α and β such that in a given position the re-
sulting digit is a "1" if and only if the corresponding digits of α
and β were "1's", otherwise the resultant digit is a "0". This order
has had its chief use in separating parts of a formed order or of muli-
ply stored data.

c. Alarm circuits.

The monitoring system consists of two independent cir-
cuits--one which observes voltage stability of the DC supplies, the
other observing whether any of the 20 associated fuses have "blown".
For each voltage there is a pair of neons, one for the stability func-
tion and one for the "fuse-blown" function. If a voltage fluctuates
beyond some predetermined amount, its stability monitor is actuated and
the associated neon will blink on and off until cleared manually. Ma-
chine operation is not inhibited but the blinking neon serves to notify
the operator that this particular voltage either fluctuated momentarily
or has changed altogether. Such an indication coincident with difficulty

can facilitate servicing. Fluctuations which occur as a result of DC turn-on are sensed but automatically cleared out. The sensitivity available is adjustable from a fraction of a volt to about 10 volts in either direction, but at present each stage is set to sense a deviation of approximately 2 volts.

The "fuse-blown" monitor has a different mode of operation in that it will immediately remove all DC from the machine if any fuse failure occurs. Additionally it will prevent DC from being applied to the machine if any fuses are "blown". In either case the neon corresponding to that fuse responsible will glow continuously. Having thus located the blown fuse and with the cause remedied, insertion of a new fuse now allows a DC turn-on. The neons referred to are arranged in pairs (one pair per voltage) on a panel which is visible from the control desk. Behind this panel are located all components necessary for operation of the system. The required wiring originates at the points being sensed and converges behind the panel terminating in cable connectors thus allowing for a convenient disconnect if required. By throwing one switch the monitor can be deprived of its ability to dump DC if found to operate unreliably.

4. Machine Operation.

    a. Drum experience.

        Our smaller drum, which was constructed in the labora-
tory (except for heads) has been in use for three years and on the
whole was proven satisfactory. Maintenance problems, however, have
markedly centered on the wire-contact relays which are used primarily
for head switching but also for some timing and logical functions. The
head relays switch millivolt signals and consequently even slight oxida-
tion of the wires and contacts affects reliability. Periodic inspec-
tions and/or replacement of groups of these relays proved unsatisfactory
because of the need for removing them physically. It was not uncommon
for one or more relays in a group to become troublesome after having
been removed, cleaned and replaced. However, similar relays which exist
in some timing and logical circuitry do not exhibit this characteristic
because they switch considerably higher voltages.

        The automatic erase circuitry which was discussed in the last
report has been very useful and essentially trouble-free. It could be
automatized further but since the new drum will soon obsolete the old,
no further effort in this direction is contemplated.

    b. Tube replacement.

        A formal program of tube replacement was undertaken in
January 1955 and continued through January 1956. Of more than 2000
tubes removed after an average of 10,000 hours running time some 93%
were found to have shorts of various degrees and/or to be below initial
emission specifications for entry into the machine and were accordingly
replaced. The tube replacement program proceeded gradually so as to

interfere a minimum with the computing schedule and also to avoid implantation of multiple troubles. Computational reliability seemed to be only remotely related to tube worth so this factor also allowed for a gradual replacement program. Since the completion of the above we have spot checked and find that perhaps 50% of the tubes replaced early in the program will not now meet initial specifications. Spot checking of tubes is a part of our preventive maintenance program but also tubes are pulled and tested quite freely if a particular unit is suspected.

c. Machine troubles.

The following information has been extracted from the operating logs for 1955 and represents those troubles which we typically encounter in one year's running. The failure sub-headings are described as follows:

Wms.--dash pickups or losses because of discriminator, amplifier or CRT malfunction.

Arith.--failures in arithmetic organ (faulty gates and toggles).

Input-output--difficulties in reading in or out to IBM (or drum) not attributable to failure of the IBM reproducer.

IBM--malfunction of IBM reproducers.

Control--failure of logical circuitry within machine (commands of when, where and how).

All failures are listed irrespective of whether they occurred during routine testing or during computation.

1955	Wms.	Arith.	Input-output	IBM	Control
Jan-Feb	11	6	9	1	6
Mar-April	9	8	4	0	6
May-June	7	4	7	3	3
July*	3	3	3	1	3
Sept-Oct	7	4	7	1	4
Nov-Dec	5	0	5	0	0
	42	25	35	6	22

*August vacation

Total: 130 machine troubles.

On the basis of approximately 220 working days per year, we had a machine difficulty once every 1.7 days, roughly distributed as indicated above.

With regard to the CRT's, we have replaced 39 from 1950 to date with 1 being replaced in 1956. The above figures are not rigorous, but do provide a general picture of the maintenance problems encountered.

      d.   Operating statistics.

Weekly time records for the period are given in Table I. For completeness the time records for previous years are also given. Results are summarized in Table II, by quarters, the last quarter of 1952 being the first for which these records were kept. With respect to all tables, the time breakdowns are defined as follows:

Routine: All time spent performing a standard set of tests preliminary to each day's operation.

Engineering: All time spent in engineering improvements or additions to the machine.

Unscheduled maintenance: All time spent in diagnosing and repairing conditions which have interrupted computation or which threaten to cause errors. Also included is bad operating time which is clearly due to machine trouble.

Operation: All other machine "on" time not accounted for by the above.

Table I.

	BASIC RECORDS					DERIVED	
Week Of	Routine	Engineering	Unscheduled Maintenance	Operation	Total	(UnM + Op) Available	(Op / Av) % Operation
27 Oct.	14.5	32.5	6.0	26.0	79.0	32.0	81
3 Nov.	11.0	22.5	6.0	41.0	80.5	47.0	87
10 Nov.	10.5	17.0	37.5	14.5	79.5	52.0	28
17 Nov.	9.5	24.0	27.5	18.0	79.0	45.5	40
24 Nov.	9.5	11.5	10.0	33.0	64.0	43.0	77
1 Dec.	10.5	8.5	9.5	51.5	80.0	61.0	84
8 Dec.	10.0	19.0	9.0	42.0	80.0	51.0	82
15 Dec.	11.0	27.5	5.5	36.0	80.0	41.5	87
22 Dec.	6.5	5.5	1.5	23.0	36.5	24.5	94
29 Dec.	-	-	- (Holiday)	-	-	-	-
4th Quarter	93.0	168.0	112.5	285.0	658.5	397.5	73
5 Jan.	9.2	18.1	26.9	25.8	80.0	52.7	49
12 Jan.	8.3	4.8	35.7	31.2	80.0	66.9	47
19 Jan.	10.1	22.5	21.8	25.6	80.0	47.4	54
26 Jan.	9.5	37.0	17.6	17.7	81.8	35.3	50
2 Feb.	8.5	36.3	6.8	28.5	80.1	35.3	81
9 Feb.	7.8	29.7	9.3	34.9	81.7	44.2	79
16 Feb.	7.8	3.9	6.1	62.2	80.0	68.3	91
23 Feb.	8.4	2.5	10.7	58.1	79.7	68.8	84
2 Mar.	8.1	0	18.6	65.6	92.3	84.2	78
9 Mar.	10.5	26.0	10.2	57.3	104.0	67.5	85
16 Mar.	12.5	6.1	0.1	85.1	103.8	85.2	99
23 Mar.	7.8	10.2	9.2	77.0	104.2	86.2	89
1st Quarter	108.5	197.1	173.0	569.0	1047.6	742.0	74
30 Mar.	7.4	6.4	4.6	69.4	87.8	74.0	94
6 Apr.	13.1	16.1	4.7	78.7	112.6	83.4	94
13 Apr.	9.1	8.2	21.5	65.1	103.9	86.6	75
20 Apr.	10.8	7.7	3.3	76.0	97.8	79.3	96
27 Apr.	9.2	11.8	3.3	87.7	112.0	91.0	95
4 May	7.3	11.4	39.1	44.1	101.9	83.2	53
11 May	9.2	2.4	44.5	47.9	104.0	92.4	52
18 May	11.9	0	11.6	80.5	104.0	92.1	87
25 May	12.7	2.0	32.9	83.6	131.2	116.5	72
31 May	8.3	8.4	7.8	82.6	107.1	90.4	91
8 June	12.3	15.7	23.9	97.3	149.2	121.2	80
15 June	11.8	9.4	5.4	105.9	132.5	111.3	95
22 June	10.8	7.4	5.5	124.0	147.7	129.5	96
2nd Quarter	133.9	106.9	208.1	1042.8	1491.7	1250.9	83

Table I. (cont'd)

	BASIC RECORDS					DERIVED	
Week Of	Routine	Engineering	Unscheduled Maintenance	Operation	Total	(UnM + Op) Available	(Op / Av) % Operation
29 June	7.2	9.3	11.3	125.2	153.0	136.5	92
6 July	12.9	3.5	19.8	99.8	136.0	119.6	83
13 July	13.3	8.6	8.5	103.8	134.2	112.3	92
20 July	8.7	3.4	11.7	124.2	148.0	135.9	91
27 July	8.0	0	3.0	57.2	68.2	60.2	95
3rd Quarter	50.1	24.8	54.3	510.2	639.4	564.5	91
Machine off for moving 1 August 1953 to 10 November 1953.							
10 Nov.	0	32.0	0	0	32.0	0	- *
16 Nov.	0	38.7	0	17.1	55.8	17.1	- *
23 Nov.	0	64.0	0	0	64.0	0	- *
30 Nov.	0	67.1	0	12.9	80.0	12.9	- *
7 Dec.	14.9	13.2	7.0	43.6	78.7	50.6	86
14 Dec.	11.9	15.5	6.8	45.8	80.0	52.6	87
21 Dec.	8.4	2.0	2.7	27.8	40.9	30.5	91
4th Quarter	35.2	232.5	16.5	147.2	431.4	163.7	90
4 Jan.	9.7	9.1	23.3	40.5	82.6	63.8	63
11 Jan.	14.3	1.0	13.0	47.5	75.8	60.5	78
18 Jan.	10.1	2.6	14.2	63.1	90.0	77.3	81
24 Jan.	8.9	16.6	0	65.6	91.1	65.6	100
1 Feb.	7.0	31.7	4.9	40.8	84.4	45.7	89
8 Feb.	9.7	8.7	2.3	63.9	84.6	66.2	96
15 Feb.	11.4	19.1	3.7	43.8	78.0	47.5	92
22 Feb.	6.2	8.3	2.6	59.9	77.0	62.5	96
1 Mar.	13.3	13.2	2.0	52.6	81.1	54.6	96
8 Mar.	11.2	12.7	11.1	54.7	89.7	65.8	83
15 Mar.	7.3	8.0	5.3	68.2	88.8	73.5	93
22 Mar.	6.5	7.3	3.3	65.8	82.9	69.1	95
1st Quarter	115.6	138.3	85.7	666.4	1006.0	752.1	88
29 Mar.	6.4	0	27.3	69.2	102.9	96.5	72
5 Apr.	10.1	5.7	7.4	57.7	80.9	65.1	88
12 Apr.	11.5	8.8	4.7	46.1	71.1	50.8	91
19 Apr.	10.4	17.7	20.0	38.3	86.4	58.3	66
26 Apr.	10.5	11.7	22.3	47.2	91.7	69.5	68
3 May	8.8	11.3	0.7	69.5	90.3	70.2	99
10 May	9.7	27.0	12.3	50.3	99.3	62.6	80
17 May	8.9	17.0	3.1	62.8	91.8	65.9	95
24 May	9.9	16.2	7.1	55.0	88.2	62.1	88
31 May	11.1	0.5	10.2	55.2	77.0	65.4	84
7 June	5.5	32.8	16.2	57.4	111.9	73.6	78
14 June	14.7	4.5	10.1	73.2	102.5	83.3	88
21 June	7.1	3.2	9.7	72.8	92.8	82.5	88
2nd Quarter	124.6	156.4	151.1	754.7	1186.8	905.8	83

* Adjustment period after move.

Table I. (cont'd)

| Week Of | BASIC RECORDS | | | | | DERIVED | |
	Routine	Engineering	Unscheduled Maintenance	Operation	Total	(UnM + Op) Available	(Op / Av) % Operation
28 June	8.4	16.7	19.1	43.1	87.3	62.2	69
5 July	11.4	5.8	8.0	45.6	70.8	53.6	85
12 July	6.6	7.1	21.9	44.4	80.0	66.3	67
19 July	0.9	73.5	0	5.6	80.0	5.6	- *
26 July	9.9	12.1	20.4	69.6	112.0	90.0	72
2 Aug.	7.7	4.8	4.1	103.4	120.0	107.5	96
9 Aug.	4.8	25.7	19.0	32.5	82.0	51.5	63
16 Aug.	1.2	47.1	4.7	27.0	80.0	31.7	85
23 Aug.	5.5	17.1	18.1	38.4	79.1	56.5	68
30 Aug.	10.3	8.8	41.7	19.2	80.0	60.9	31
6 Sept.	9.8	5.7	3.2	40.3	64.0	48.5	83
13 Sept.	7.2	4.7	25.8	52.0	89.7	77.8	67
20 Sept.	11.6	10.8	21.3	64.4	108.1	85.7	75
27 Sept.	10.8	1.4	29.3	72.1	113.6	101.4	71
3rd Quarter	106.1	241.3	241.6	657.6	1246.6	899.2	73
4 Oct.	5.1	3.6	14.8	89.4	112.9	104.2	85
11 Oct.	6.7	0	27.4	66.6	100.7	94.0	71
18 Oct.	10.7	3.3	11.3	97.2	122.5	108.5	89
25 Oct.	6.4	4.5	5.5	101.0	117.4	106.5	95
1 Nov.	7.1	10.4	0.3	101.1	118.9	101.4	99
8 Nov.	5.0	17.8	2.4	73.3	98.5	75.7	97
15 Nov.	6.6	21.8	7.1	74.5	110.0	81.6	91
22 Nov.	7.0	4.2	7.4	58.5	77.1	65.9	89
4 Dec.	4.8	29.5	2.9	49.8	87.9	52.7	94
10 Dec.	6.6	39.4	0.9	51.1	98.0	52.0	98
17 Dec.	3.7	34.7	6.4	37.2	82.0	43.6	85
24 Dec.	5.6	7.3	3.1	45.3	61.3	48.4	94
4th Quarter	75.3	145.5	89.5	845.0	1187.2	988.5	94
3 Jan.	10.9	14.8	14.2	43.8	83.7	58.0	75
10 Jan.	5.6	31.0	0.3	33.6	70.5	33.9	99
17 Jan.	3.7	24.1	25.1	22.0	74.9	47.1	46
24 Jan.	11.3	22.0	15.8	28.7	77.8	44.5	64
31 Jan.	10.6	2.7	10.5	24.5	48.3	35.0	70
7 Feb.	8.1	5.0	6.9	31.6	51.6	38.5	82
14 Feb.	6.8	12.8	15.8	46.1	81.5	61.9	74
21 Feb.	7.1	10.3	7.6	58.4	83.4	66.0	88
28 Feb.	9.9	2.6	2.2	71.4	86.1	73.6	97
7 Mar.	6.6	10.7	17.3	46.2	80.8	63.5	72
14 Mar.	7.4	30.8	2.5	34.7	75.4	37.2	93
21 Mar.	7.4	9.8	5.5	39.6	62.3	45.1	87
28 Mar.	8.4	2.0	16.3	47.3	74.0	63.6	74
1st Quarter	103.8	178.6	140.0	527.9	950.3	667.9	79

* Air conditioning installed.

Table I. (cont'd)

Week Of	BASIC RECORDS					DERIVED	
	Routine	Engineering	Unscheduled Maintenance	Operation	Total	(UnM + Op) Available	(Op / Av) % Operation
4 Apr.	7.2	11.4	9.2	32.4	60.2	41.6	78
11 Apr.	6.4	26.1	7.7	39.8	80.0	47.5	84
18 Apr.	4.9	4.2	31.2	38.6	78.9	69.8	55
25 Apr.	6.3	3.1	29.2	44.5	83.1	73.7	60
2 May	3.8	0.6	37.3	36.6	78.2	73.9	49
9 May	4.5	1.95	55.6	23.3	85.4	78.9	29
15 May	5.2	13.6	48.2	12.2	79.2	60.4	20
23 May	6.3	4.7	20.1	49.1	80.1	69.2	71
30 May	5.2	1.0	33.1	23.7	62.9	56.8	42
6 June	7.8	0.7	8.2	69.3	86.1	77.5	89
13 June	5.9	10.4	4.9	59.1	80.3	64.0	92
20 June	9.3	15.0	19.4	35.3	78.9	54.7	65
27 June	8.0	8.9	4.0	60.4	81.3	64.4	94
2nd Quarter	80.8	101.65	308.1	524.3	1014.6	832.4	63
4 July	5.4	3.5	9.9	47.3	66.1	57.2	83
11 July	9.7	0.9	8.3	66.8	85.7	75.1	89
18 July	9.2	10.1	13.2	67.1	96.4	80.3	84
25 July	5.8	2.6	22.2	66.7	97.2	88.9	75
1 Aug.	9.0	1.5	12.3	71.8	94.5	84.1	85
Vacation 6 August to 6 September.							
6 Sept.	0	32.0	0	0	32.0	0	-
12 Sept.	7.4	7.5	38.3	23.7	76.9	62.0	38
19 Sept.	5.1	19.6	1.1	46.3	72.0	47.4	97
26 Sept.	8.8	19.3	10.9	40.4	79.4	51.3	78
3rd Quarter	60.4	97.0	116.2	430.1	701.1	546.3	79
2 Oct.	6.7	0	45.8	33.7	86.2	79.5	42
9 Oct.	4.5	8.0	32.8	35.9	81.2	68.7	52
17 Oct.	6.1	2.9	27.7	39.2	75.9	66.9	58
24 Oct.	5.8	2.2	13.9	59.4	81.3	73.3	81
31 Oct.	6.7	5.8	5.6	61.5	79.6	67.1	92
7 Nov.	5.9	2.4	13.7	57.8	79.8	71.5	81
14 Nov.	6.9	2.5	4.3	65.4	79.1	69.7	94
21 Nov.	5.1	2.1	0.8	56.0	63.9	56.8	98
28 Nov.	8.6	7.4	2.9	59.0	77.9	61.9	95
5 Dec.	6.6	23.4	0	40.1	70.2	40.1	100
12 Dec.	9.8	4.6	1.1	62.7	78.3	63.8	98
19 Dec.	6.0	18.4	1.5	39.2	65.2	40.7	96
4th Quarter	78.7	79.7	150.1	609.9	918.6	760.0	80

Table I.

	BASIC RECORDS					DERIVED	
Week of	Routine	Engineering	Unscheduled Maintenance	Operation	Total	(UnM + Op) Available	(Op / Av) % Operation
3 Jan.	6.7	1.7	10.6	42.6	61.8	53.2	80
9 Jan.	6.6	4.4	5.7	64.3	81.0	70.0	92
16 Jan.	10.0	8.5	.3	51.5	70.3	51.8	99
23 Jan.	5.6	14.9	0	58.9	79.5	58.9	100
30 Jan.	0	56.1	1.7	0	57.8	1.7	-
6 Feb.	4.6	47.0	15.8	12.5	79.8	28.3	44
13 Feb.	4.5	16.7	.9	60.7	82.7	61.8	98
20 Feb.	2.9	21.9	1.6	63.4	89.9	65.0	97
27 Feb.	4.5	29.0	1.0	43.3	77.8	44.3	97
5 Mar.	7.3	7.3	12.3	48.5	75.4	60.8	79
12 Mar.	6.7	9.5	1.8	58.5	76.5	60.3	97
19 Mar.	6.0	5.6	5.5	47.1	64.1	52.6	89
26 Mar.	6.2	10.7	.08	46.9	63.9	47.0	99
1st Quarter	71.6	233.3	57.28	598.2	960.3	655.7	89
2 Apr.	9.5	19.6	.7	59.2	89.0	59.9	98
9 Apr.	6.8	10.8	3.0	51.7	72.4	54.7	94
16 Apr.	6.7	17.2	19.3	40.1	83.4	59.4	67
23 Apr.	10.1	24.4	22.3	32.9	90.8	55.2	59
30 Apr.	6.0	22.6	15.1	38.6	82.4	53.7	71
14 May	11.2	16.8	8.5	53.7	90.3	62.7	85
21 May	3.7	33.5	7.0	46.0	90.9	53.6	86
28 May	2.7	20.1	8.7	26.4	57.9	35.1	75
4 June	14.9	26.0	6.6	56.9	104.5	63.5	89
11 June	8.2	26.8	6.9	56.0	97.9	62.9	89
18 June	9.0	35.1	5.6	39.7	89.5	45.3	87
25 June	8.7	4.6	12.4	64.4	90.2	76.8	83
2nd Quarter	97.5	257.5	116.1	566.2	1039.2	682.8	82
2 July	15.4	5.5	16.0	65.2	102.1	81.2	80
9 July	7.9	14.0	7.4	120.3	149.7	127.7	94
16 July	1.9	13.3	14.3	92.7	122.2	107.0	86
23 July	6.3	6.6	14.8	90.5	118.2	105.3	85
Vacation	August 4-September 4						
4 Sept.	3.7	.7	.3	7.1	11.9	49.0	95
10 Sept.	4.7	15.4	4.0	10.3	34.5	14.3	72
17 Sept.	4.2	13.6	15.9	3.8	37.6	19.7	23
24 Sept.	1.1	0	3.2	4.4	8.8	7.6	57
3rd Quarter	45.2	69.1	75.9	394.3	585.0	470.2	84
1 Oct.	Week of Eng. 3" & 5" memory adjustments						
8 Oct.	1.7	2.3	27.4	1.6	33.1	29.0	5
15 Oct.	3.1	6.6	15.8	11.5	37.2	27.3	42
22 Oct.	2.2	20.5	2.4	21.8	47.0	24.2	90
29 Oct.	3.1	26.4	2.0	25.1	56.7	27.1	92
4 Nov.	4.3	20.5	22.8	19.8	67.6	42.6	46

Table I. (Cont'd)

	BASIC RECORDS					DERIVED	
Week of	Routine	Engineering	Unscheduled Maintenance	Operation	Total	(UnM + Op) Available	(Op / Av) % Operation
11 Nov.	5.4	19.3	4.3	37.9	67.0	42.6	89
19 Nov.	2.9	13.9	5.4	46.2	68.7	51.6	89
25 Nov.	2.6	14.8	1.9	92.5	111.8	94.4	97
3 Dec.	4.0	14.0	20.4	26.9	65.3	47.3	57
10 Dec.	2.6	14.0	15.9	37.3	69.8	53.2	70
17 Dec.	1.6	20.8	.8	52.9	76.2	53.7	98
4th Quarter	33.5	173.1	119.1	373.5	699.7	492.6	76

Table II.

Quarter	BASIC RECORDS					DERIVED	
	Routine	Eng.	Unsched. Maint.	Operation	Total	(UnM + OP) Available	(Op / Av) % Operation
1952							
4th	93.0	168.0	112.5	285.0	658.5	397.5	73
1953							
1st	108.5	197.1	173.0	569.0	1047.6	742.0	74
2nd	133.9	106.9	208.1	1042.8	1491.7	1250.9	83
3rd	50.1	24.8	54.3	510.2	639.4	564.5	91
4th	35.2	232.5	16.5	147.2	431.4	163.7	90
1954							
1st	115.6	138.3	85.7	666.4	1006.0	752.1	88
2nd	124.6	156.4	151.1	754.7	1186.8	905.8	83
3rd	106.1	241.3	241.6	657.6	1246.6	899.2	73
4th	75.3	145.5	89.5	845.0	1187.2	988.5	94
1955							
1st	103.8	178.6	140.0	527.9	950.3	667.9	79
2nd	80.8	101.65	308.1	524.3	1014.6	832.4	63
3rd	60.4	97.0	116.2	430.1	701.1	546.3	79
4th	78.7	79.7	150.1	609.9	918.6	760.0	80
1956							
1st	71.6	233.3	57.28	598.2	960.3	655.7	89
2nd	97.5	257.5	116.1	566.2	1039.2	682.8	82
3rd	45.2	69.1	75.9	394.3	585.0	470.2	84
4th	33.5	173.1	119.1	373.5	699.7	492.6	76

ADDENDA

The following facilities have been added to the machine while this report was in preparation:

(i) <u>A spill-indicator chassis</u> detects spills which may have occured as a result of left shift or of addition. A new transfer order inspects the state of the spill toggle and will cause transfer or not dependent on the state of the spill toggle.

(ii) <u>A drum write-inhibition circuit</u> has been installed which permits any quarter(s) of our 16384-word drum to be preserved as a library of sub-routines or test codes etc. Reading from the inhibited quarter(s) is permitted, but if writing is attempted the external control simply "hangs" and no information is transferred.

(iii) <u>The IBM-read-punch circuitry</u> has been incorporated into the external control which was designed for the new drum. This new IBM mode allows for the use of one external order to command all input-output media (i.e. drum, IBM and, later, tapes if desired). The old drum IBM control is not used at all now and is being removed from the machine.
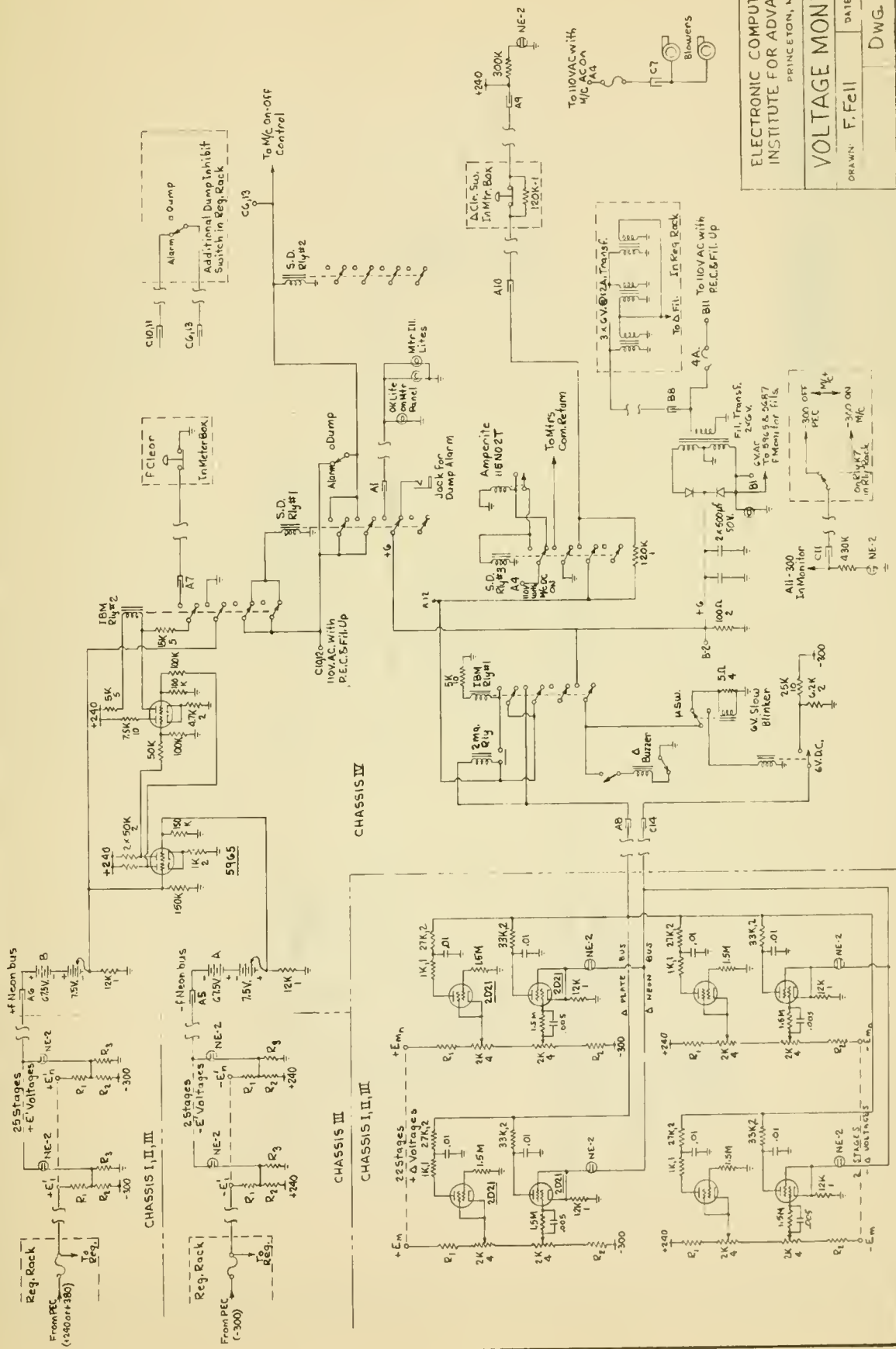
ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N.J.

VOLTAGE MONITORING

DRAWN F. Fell   DATE: 4-28-55

DWG. No. A-2024
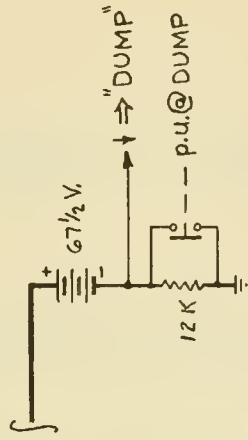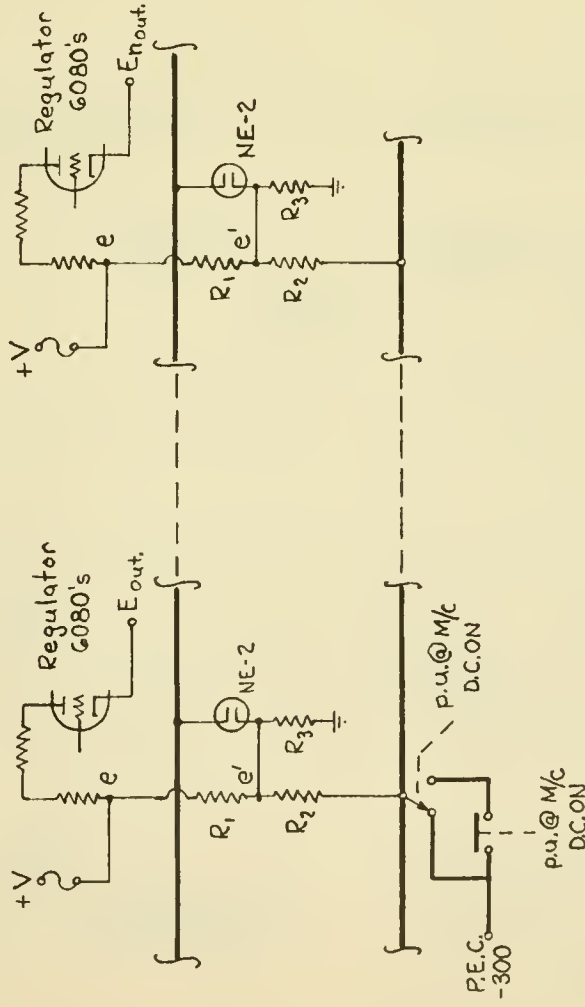
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INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.

TYPICAL STAGE - FUSE MONITOR'G

DRAWN: F Fell | DATE: 1-19-56

SCALE: | Dwg. No. A = 2030

* R.47 *

* D47 ○

○ C47

2^0 2^{-7} 2^{-8} 2^{-14} 2^{-21} 2^{-22} 2^{-29}

ER   ER   ER

D'47 ○

To DIODE SOCKETS

○ R³47

2^{-15} 2^{-22} 2^{-23} 2^{-30}

I'47 ○

ER   ER

.T'47 ○

To DIODE SOCKETS

○ C'47

47SP ○

2^{-16} 2^{-22} 2^{-23} 2^{-29}

○ 47SP.

47SP ○

EC   ← CARRY   EC

47SP ○

D24 ○
I14 ○
T14 ○
G14 ○

CTRL   CTRL

○ C24

○ M/c47

EXTERNAL ORDERS

| $2^0 2^{-1}$ | STARTING ADRESS | $2^{-14} 2^{-15} 2^{-16}$ | No. OF EVENTS | $2^{-17} 2^{-30}$ | T | D | I | $2^{-34} 2^{-35}$ | M | T | D | I | G | M |

To θ CTR ETC.   To E.C.   S   R
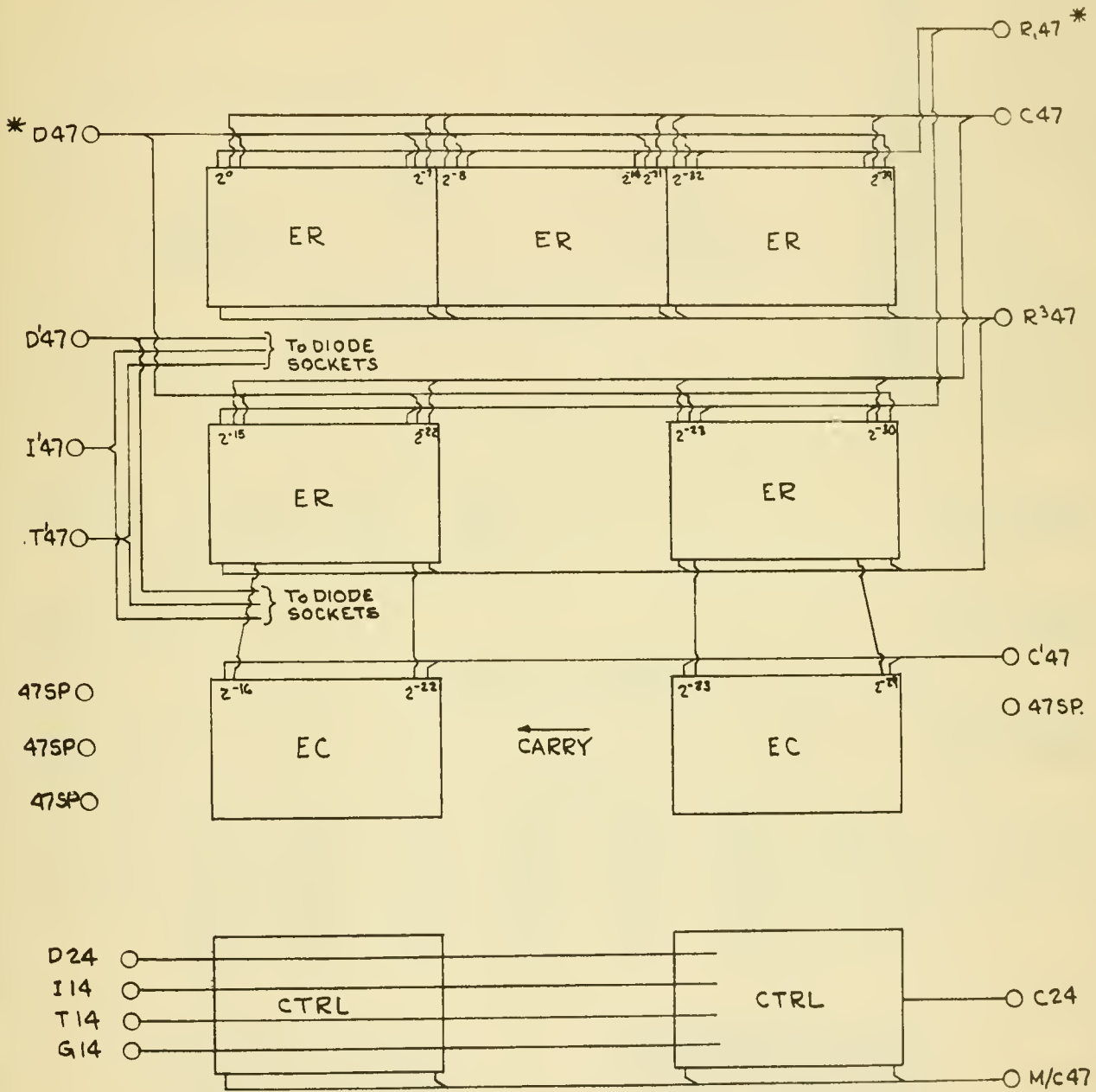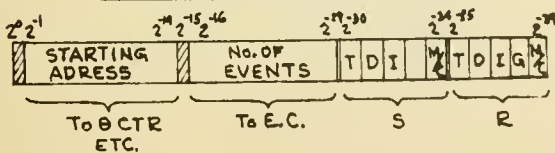
* See Dwg.No.A-   for Terminal Designations

ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N.J.

EXT. CAB'N'T-SIGNAL WIRES

Dwn. F.Fell
Date: 10-7-55

DWG. No. A-2549

iR_N Input

ER_{N+1} Input

Hughes IN 117

1 10 11 12 13 14 15 16

9 10 11 12 13 14 15 16

2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

D_N
T_N
I_N

I_{N+1}
T_{N+1}
D_{N+1}
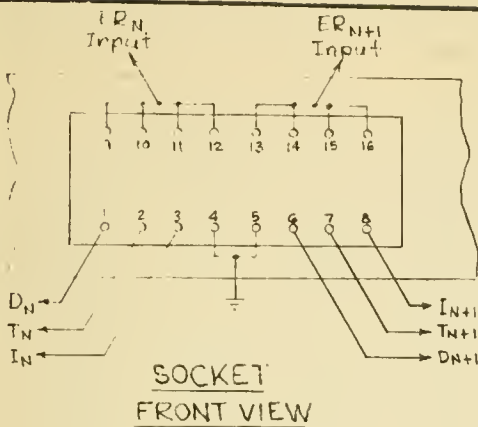
SOCKET
FRONT VIEW
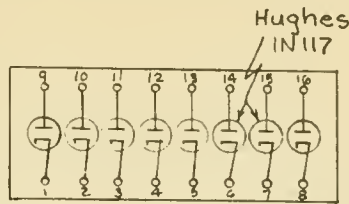
PLUG
FRONT VIEW

DIGIT INPUT DIODES

IBM I'47 — (47) M

(47) SP   (47) SP   (47) SP

(24) M — Cons. C24

TAPE T'47 — (47) F

(47) F — M/C M/C47

DRUM D'47 — (47) M

TOP VIEW

(47) M — R^3 $R^3$47

DRUM D47 — (47) F

FRONT

(47) F — R_1 $R_1$47

M (14)   F (14)   M (14)   F (14)   (47)   F (47)   M (47)

DRUM D24   IBM I14   GRAPH G14   TAPE T14   V-E   CONS. C'47   CONS. C47
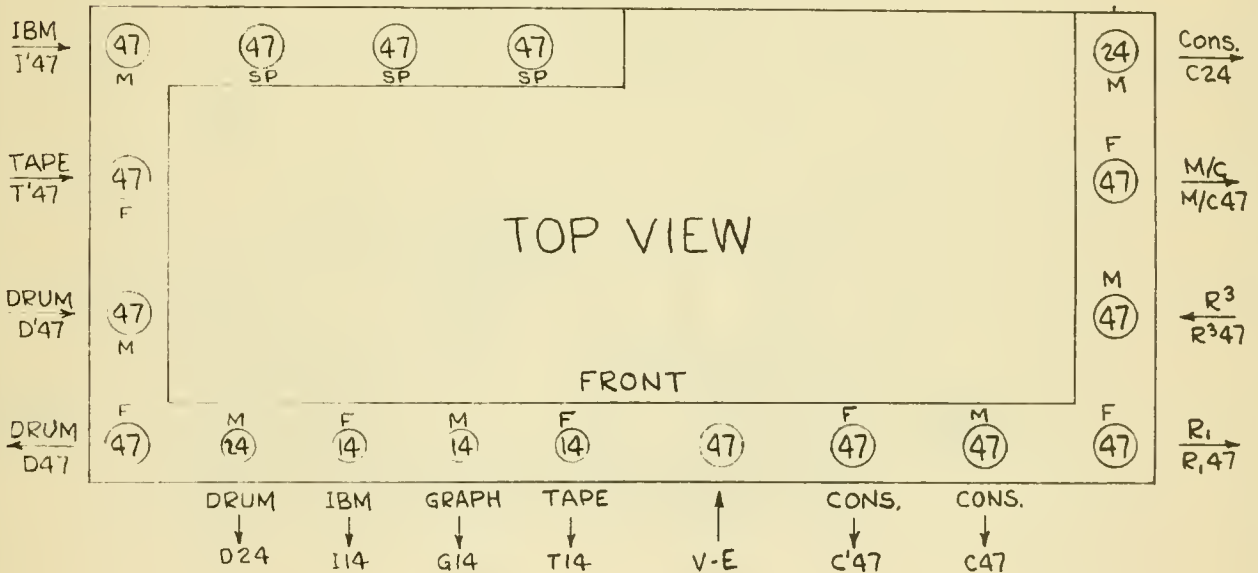
CONNECTOR	FUNCTION
I'47	Digits from IBM
T'47	Digits from TAPE
D'47	Digits from DRUM
D47	Digits to D,T,I,G
D24	CTRL to DRUM
I14	CTRL to IBM
G14	CTRL to GRAPH
V-E	Volts from Rly R.

CONNECTOR	FUNCTION
T14	CTRL to TAPE
C47	ER Neons to CONS
$R_1$47	Digits to R_1
$R^3$47	Digits from R^3
M/C47	CTRL to M/C
C24	CTRL, Neons to CONS
C'47	EC Neons to CONS

CONNECTOR LAYOUT

FilA ← | E.R. | E.R. | E.R. | → FilA

E.R.   E.R.

E.C.   E.C.

CTRL   CTRL

↓ FilB   ↓ Fil.C

Rly −300   Rly +150   Rly +110   −150 8μf 600   Blwr outlet   Rly φ3   Rly φ2   Rly φ1

+110 8μf 600

−300 8μf 600

Variacs

FilB 12v.@36A.   ½ Fil.A 12v.@12A.   ½ FilA 12v.@12A. →   Fil.C 12v.@36A.

↓ φ1 PRI.   ↓ φ2 PRI   ↓ φ3 PRI

φ1   φ2   φ3

Fil. C.T. Plug
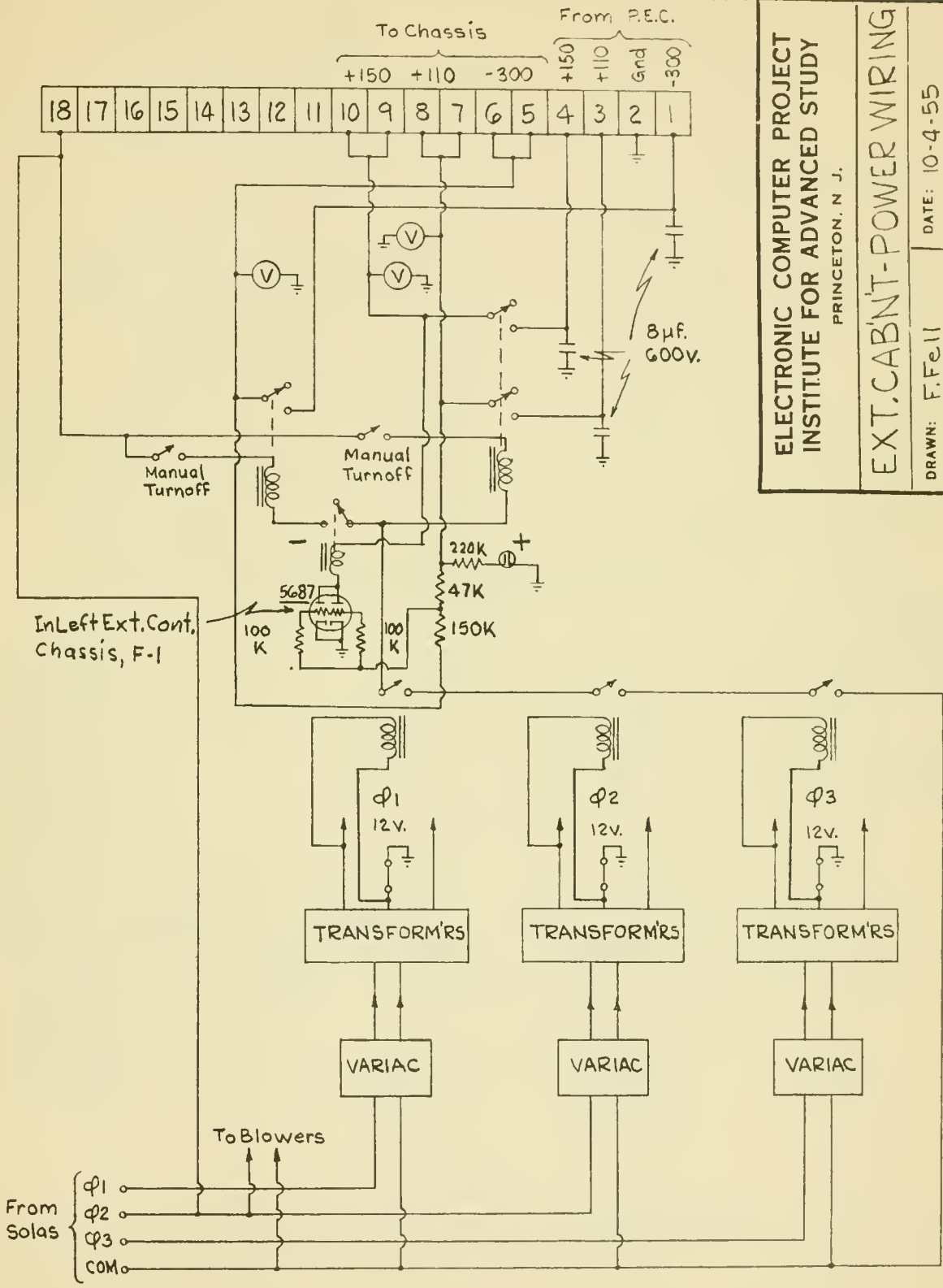
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INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.

EXT. CAB'NT - POWER WIRING

DRAWN: F. Fell | DATE: 10-4-55

Dwg. No. A-2552

SCALE

Electronic Computer Project
Institute for Advanced Study
Princeton, N.J.

DRUM CABNT-POWER WIRING

DWG. No. A-259

DRWN F. Fell

DATE 12-21-55
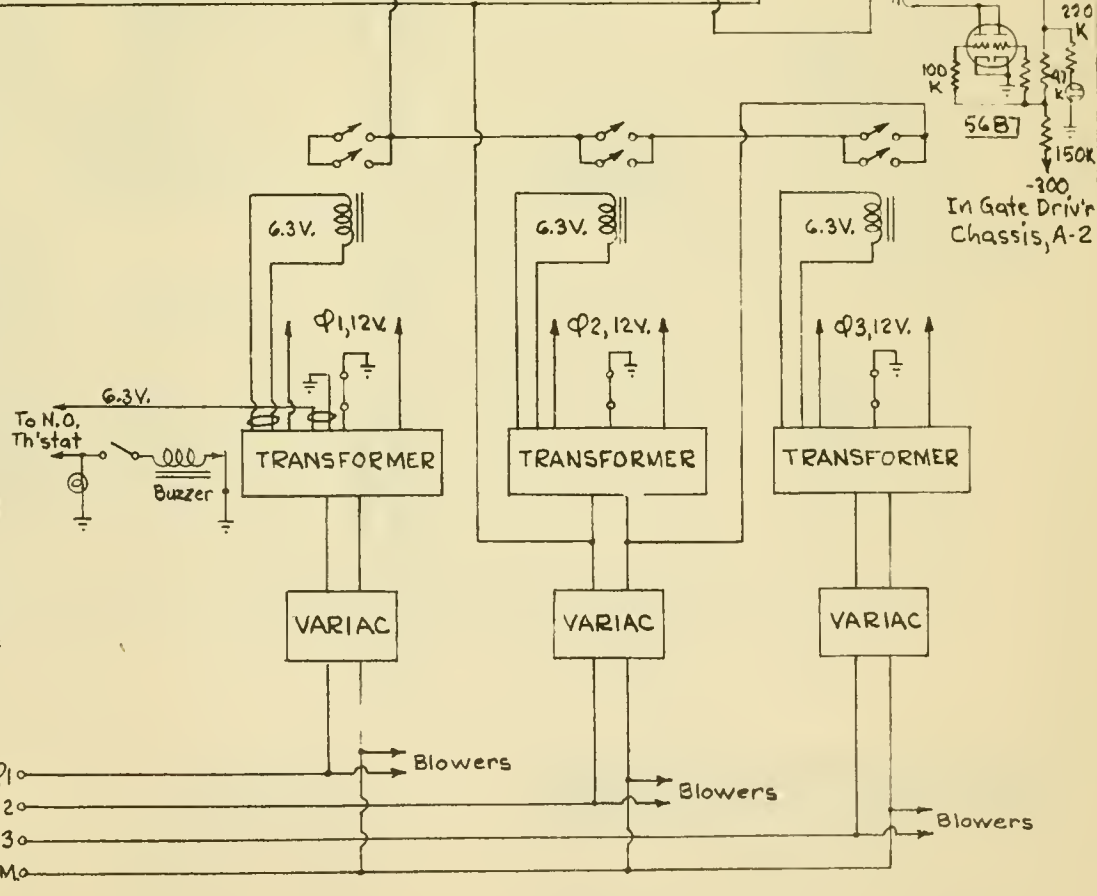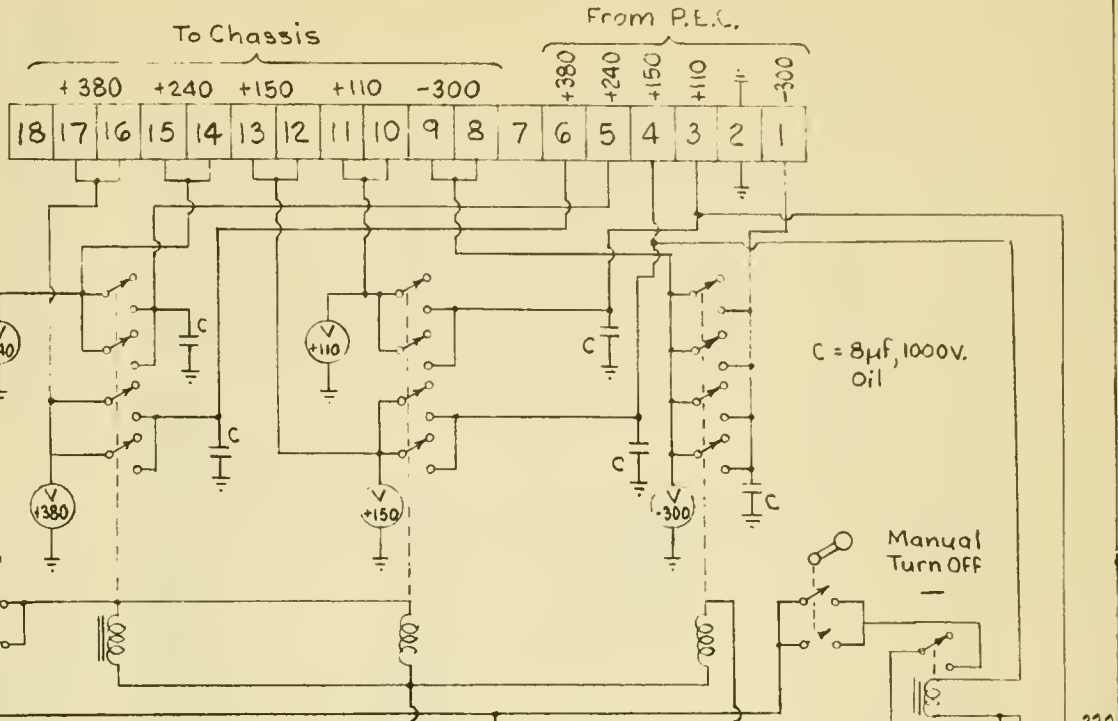
ELECTRONIC COMPUTER PROJECT
INSTITUTE FOR ADVANCED STUDY
PRINCETON, N J.

DRUM CAB'NT-LAYOUT

DRWN F. FELL

DATE 12-22-55

Dwg No. A-2561

On Digit Repeater Chassis

ELECTRONIC COMPUTER PROJECT
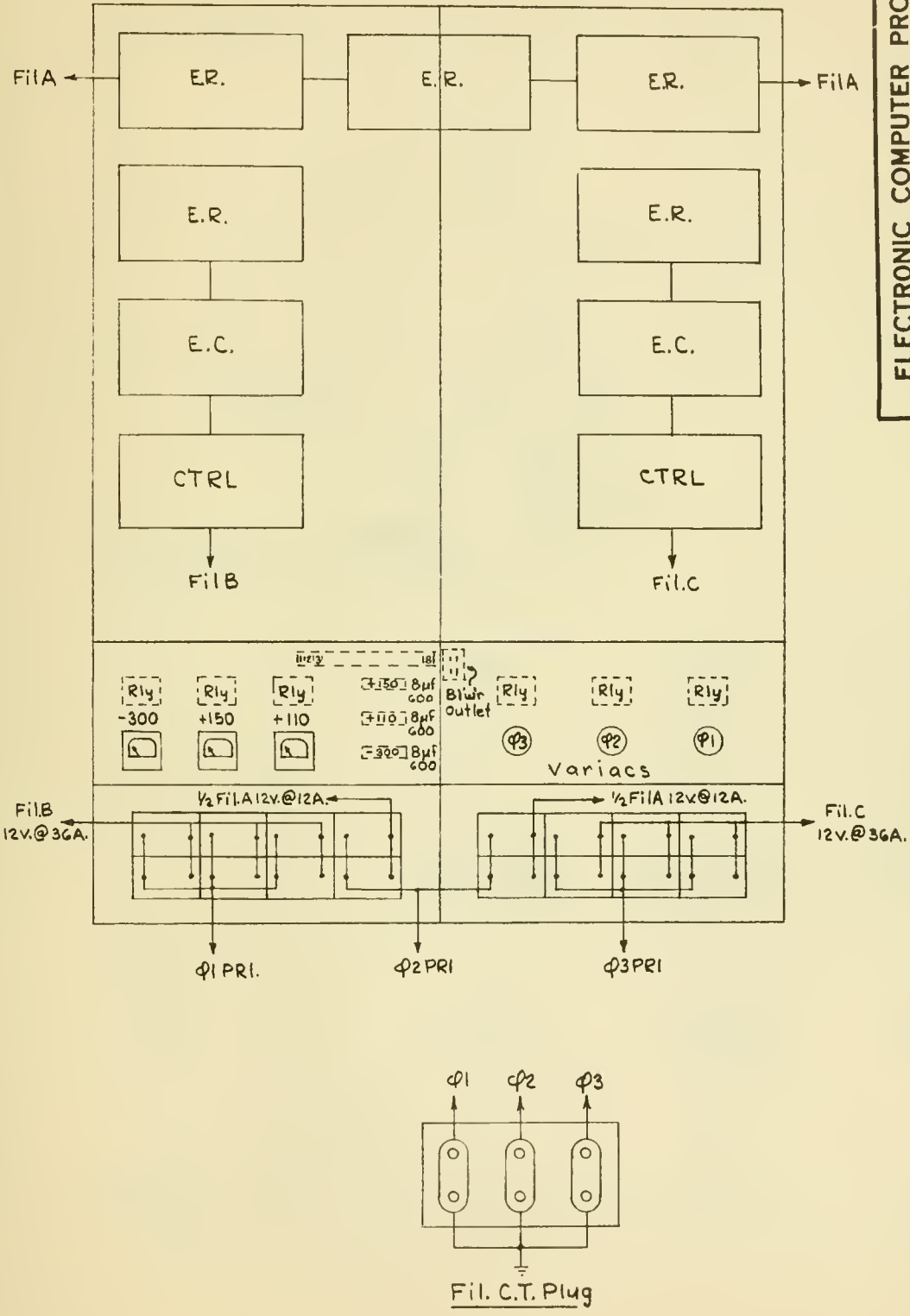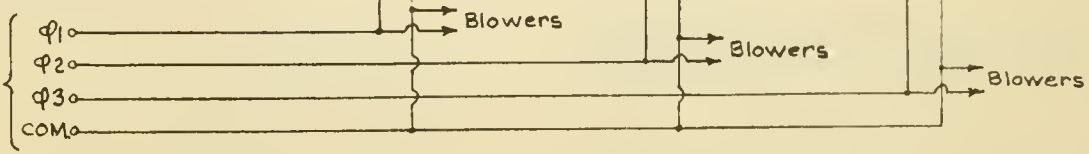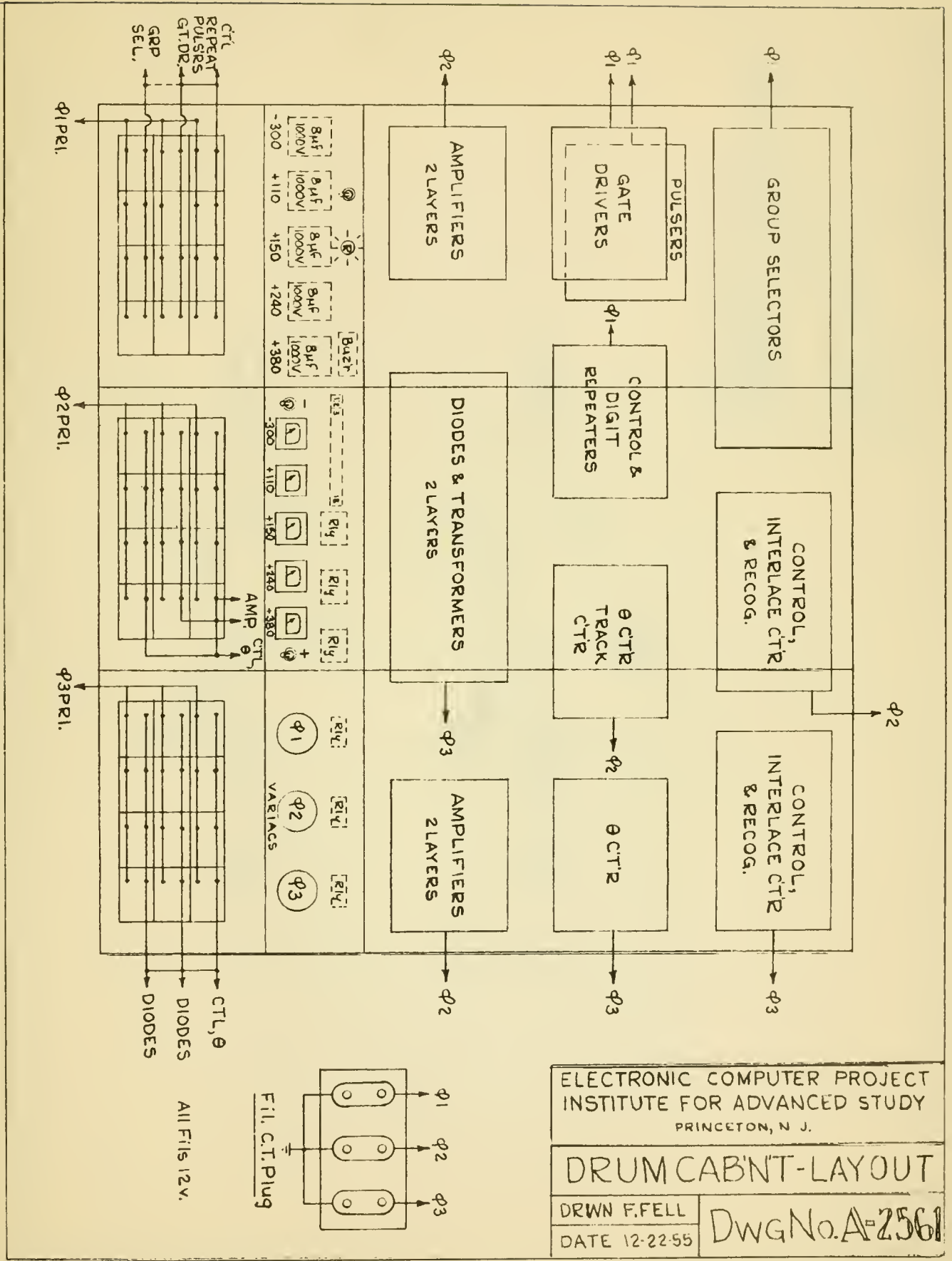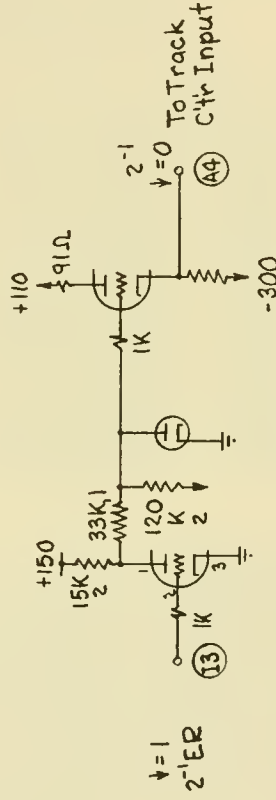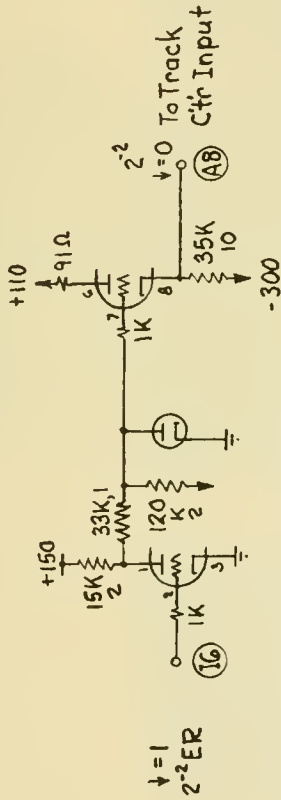INSTITUTE FOR ADVANCED STUDY
PRINCETON, N. J.

DIGIT INVERTERS FOR TRACK
COUNTER INPUT

DRAWN: F. Fell   DATE: 1-13-56

SCALE: DWG. No. A=2566

DIODES-TRANSFORMERS

AMPLIFIERS	A	B	C	D		A	B	C	D	AMPLIFIERS
0	O	O	O	O		O	O	O	O	10
1	O	O	O	O		O	O	O	O	11
2	O	O	O	O		O	O	O	O	12
3	O	O	O	O		O	O	O	O	13
4	O	O	O	O		O	O	O	O	14
5	O	O	O	O		O	O	O	O	15
6	O	O	O	O		O	O	O	O	16
7	O	O	O	O		O	O	O	O	17
8	O	O	O	O		O	O	O	O	18
9	O	O	O	O		O	O	O	O	19

FRONT PANEL·FRONT VIEW

DIODES-TRANSFORMERS

AMPLIFIERS	A	B	C	D		A	B	C	D	AMPLIFIERS
20	O	O	O	O		O	O	O	O	30
21	O	O	O	O		O	O	O	O	31
22	O	O	O	O		O	O	O	O	32
23	O	O	O	O		O	O	O	O	33
24	O	O	O	O		O	O	O	O	34
25	O	O	O	O		O	O	O	O	35
26	O	O	O	O		O	O	O	O	36
27	O	O	O	O		O	O	O	O	37
28	O	O·O	O			O	O·O	O		38
29	O	O	O	O		O	O	O·O		39

REAR PANEL·REAR VIEW

e.g. This would be Group B #38 = Head # I-5

	1	2	3	4	5	6	7	8	9	10	11
P	D25	A20	B20	C20	C35	D20	D19	D18	D17	D16	D15	X
O	D26	A21	B21	C21	C34	D21	C10	C0	B0	A0	D14	X
N	D27	A22	B22	C22	C33	D22	C11	C1	B1	A1	D13
M	D28	A23	B23	C23	C32	D23	C12	C2	B2	A2	D12
L	D29	A24	B24	C24	C31	D24	C13	C3	B3	A3	D11
K	D30	A25	B25	C25	C30	C36	C14	C4	B4	A4	D10
J	D31	A26	B26	C26	B39	C37	C15	C5	B5	A5	D9
I	D32	A27	B27	C27	B38	C38	C16	C6	B6	A6	D8
H	D33	A28	B28	C28	B37	C39	C17	C7	B7	A7	D7
G	D34	A29	B29	C29	B36	B19	C18	C8	B8	A8	D6
F	D35	"B"	"B"	A39	B35	B18	C19	C9	"B"	A9	D5
E	D36	"O"	"O"	A38	B34	A19	B17	B13	"O"	"O"	D4
D	D37	"S"	"S"	A37	B33	A18	B16	B12	"S"	"S"	D3
C	D38	"T"	"T"	A36	B32	A17	B15	B11	"T"	"T"	D2
B	D39	A30	A32	A35	B31	A16	B14	B10	B9	A10	D1
A	A31	A33	A34	B30	A15	A14	A13	A12	A11	D0	

DRUM HEADS

DRUM HEADS MAPPING

GROUP A (00)		GROUP B (01)		GROUP C (10)		GROUP D (11)	
STAGE	HEAD	STAGE	HEAD	STAGE	HEAD	STAGE	HEAD
0	0-10	0	0-9	0	0-8	0	A-10
1	N-10	1	N-9	1	N-8	1	B-11
2	M-10	2	M-9	2	M-8	2	C-11
3	L-10	3	L-9	3	L-8	3	D-11
4	K-10	4	K-9	4	K-8	4	E-11
5	J-10	5	J-9	5	J-8	5	F-11
6	1-10	6	I-9	6	I-8	6	G-11
7	H-10	7	H-9	7	H-8	7	H-11
8	G-10	8	G-9	8	G-8	8	I-11
9	F-10	9	B-9	9	F-8	9	J-11
10	B-10	10	B-8	10	0-7	10	K-11
11	A-9	11	C-8	11	N-7	11	L-11
12	A-8	12	D-8	12	M-7	12	M-11
13	A-7	13	E-8	13	L-7	13	N-11
14	A-6	14	B-7	14	K-7	14	0-11
15	A-5	15	C-7	15	J-7	15	P-11
16	B-6	16	D-7	16	I-7	16	P-10
17	C-6	17	E-7	17	H-7	17	P-9
18	D-6	18	F-6	18	G-7	18	P-8
19	E-6	19	G-6	19	F-7	19	P-7
20	P-2	20	P-3	20	P-4	20	P-6
21	0-2	21	0-3	21	0-4	21	0-6
22	N-2	22	N-3	22	N-4	22	N-6
23	M-2	23	M-3	23	M-4	23	M-6
24	L-2	24	L-3	24	L-4	24	L-6
25	K-2	25	K-3	25	K-4	25	P-1
26	J-2	26	J-3	26	J-4	26	0-1
27	I-2	27	I-3	27	I-4	27	N-1
28	H-2	28	H-3	28	H-4	28	M-1
29	G-2	29	G-3	29	G-4	29	L-1
30	B-2	30	A-4	30	K-5	30	K-1
31	A-1	31	B-5	31	L-5	31	J-1
32	B-3	32	C-5	32	M-5	32	I-1
33	A-2	33	D-5	33	N-5	33	H-1
34	A-3	34	E-5	34	0-5	34	G-1
35	B-4	35	F-5	35	P-5	35	F-1
36	C-4	36	G-5	36	K-6	36	E-1
37	D-4	37	H-5	37	J-6	37	D-1
38	E-4	38	I-5	38	I-6	38	C-1
39	F-4	39	J-5	39	H-6	39	B-1

"S"
D-2
D-3
D-9
D-10

"O"
E-2
E-3
E-9
E-10

"T"
C-2
C-3
C-9
C-10

"B"
F-2
F-3
F-9

22K

Adder

2^n

R_1 ↓ =1

1N117

40 Wire Cable
To Cannon 47

R₁ Input From E.R.
To M/C.

33K

R^3

+110

100   ≥100

1K   1K

5965

7   8

3   6

2^n 2^{n+1}

40 Wire Cable
To E.R. Input
via Cannon 47
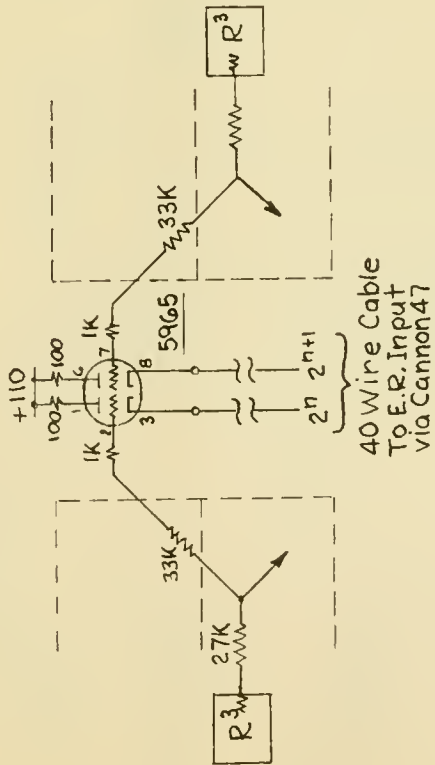
R³ Cathode Followers
From M/C to E.R.

33K

27K

R^3

External Digit Processing
in Machine (general)
2 Nov 55 JP

* needed for combined drums

AUTOMATIC ERASE
2/3/55